Total Power Data Interface

Design Considerations

Mick Brooks, August 11, 2000

Revision History:

2000-8-11: Comments from Systems Group incorporated
2000-7-26: Minor comments after Computing group discussion
2000-7-19: Added discussion of Ethernet option; reversed recommendation to CAN interface
2000-7-7: Included additional comments by D'Addario
2000-6-27: Fixed up numbers of detectors again as suggested by D'Addario and Brundage
2000-6-23: Fixed up numbers of detectors and other stuff as suggested by Stauffer and Glendenning
2000-6-21: Initial revision for comment

1 Introduction

The purpose of this document is to investigate the implementation possibilities for the collection of total power data samples from the IF Down-converter subsystem at an antenna. Although this data is science data, it will not be transmitted on the science data transmission system. Instead, the Monitor and Control System is responsible for collecting the data and transmitting them to the central control building for archiving.

It is not intended that this document provide a complete specification of the interface proposed; this task is left until a decision to proceed is made. An ICD and design documentation can then attend to the remaining unresolved issues.

The organization of this document is as follows. Section 2 describes some general principles which should guide the selection of a suitable implementation solution. The basic requirements of the interface are examined in Section 3 and some possible implementation solutions are compared in Section 4. The final section describes the ALMA Computing Group's preferred solution in more detail and examines some of the outstanding questions.

2 Design Principles

- Minimize number of interfaces to support

At present, the M&C system uses a simple application-level protocol over a CAN bus. The prototype correlator intends to use a CAN bus system similar to this for internal

communications. There will also be Ethernet and ATM interfaces between non-real-time components of the Computing System.

While it is desirable to keep hardware and interface variations within the project to a minimum it is recognized that the total power interface could add another.

- Use off-the-shelf or previously developed hardware if possible to speed development time

The delivery of the test interferometer electronics is scheduled for August 2001. The need for rapid development to meet this deadline would tend to indicate that the purchase of commercial solutions, or at least the minimization of new development work, should be pursued.

- Try to make the test interferometer interface as close to the production system interface as possible

The intention for the test interferometer is to develop true prototypes for hardware to be used in the final array. Any selected solution should be able to cope with the projected requirements of the final array, at least in so far as these can be estimated at the present time.

3 Interface Requirements

3.1 Physical interconnection

The IF Down-converter subsystem will be located in the analog rack situated in the receiver cabin. In order to minimize the effects of RF noise, the total power signals should be digitized within this subsystem.

A digital interface, therefore, is needed between the Down-converter subsystem and the VME single board computer (known in Computing Section terminology as the ABM) in the digital rack.

Assuming the ABM is in the digital rack in the receiver cabin implies that the length of such a digital connection will be no less than 2 meters and no more than 4.5 meters. If the ABM is situated on the external platform this number will be greater as the connection will have to be run through the elevation wrap, but it should still not exceed 10 meters.

This position of the ABM and hence the distance between down-converter and ABM is not expected to change significantly for the production antennas.

3.2 Data Rates

For the test interferometer (TI), we will have 6 samplers. These are the full bandwidth at two polarizations and one sampler for each baseband. It is not yet clear whether a 16 bit

sample will be enough; we should allow for 24 bit samples just in case. The sampling interval will be two milliseconds. This leads to a total data rate of 18 bytes every 2 milliseconds or 72 kbps.
For the production array we will have double sideband signals, still with dual polarizations, the data rate doubles to 144 kbps. All of the proposed solutions in Section 4 have sufficient bandwidth for both the TI and the production array data rates.

4 Design Options

4.1 Use a dedicated CAN bus

A design which would achieve great reuse is to dedicate a single CAN bus to the total power data. This bus would have a single node which would generate the data. Actual data throughput of a 1 Mbps CAN approaches 600 kbps which is more than adequate for this application.

The length limitation for a CAN bus operating at 1 Mbps of 40 m is likewise not an issue regardless of the location of the ABM.

Advantages

- Possibly reuse AMBSI at device end of link, but still need analog-to-digital converters
- Reuse software and hardware at ABM end of link
- SPI port of AMBSI is available for interfacing to A/D converters
- Inherently multi-drop, so that the addition of a second down-converter for the production system is handled transparently

Disadvantages

- Will generate over 1500 interrupts per second on the ABM; on the MVME2700 processor planned for use as the ABM this load has been measured at about 10% loading on the CPU. The interrupt load accounts for about 4%.
- Requires specific code in AMBSI for this application, although CAN code will be reused at both the AMBSI and ABM

4.2 A dedicated synchronous serial port

This design could reuse the AMBSI hardware or a similar micro-controller based design but would not use a CAN bus but rather the High Speed Synchronous Serial port of the C167 micro-controller. This port is capable of data throughput up to 5Mbps and with the correct transceivers the length is not an issue.

The two signals (one data and one clock) would be transmitted by twisted pair RS422 to the ABM. The ABM can use an MVME761 transition module and existing Serial Communications Controller hardware on the motherboard to sink the data.

Advantages

- Reuse AMBSI at device end of link, but still need serial drivers and analog-to-digital converters
- Use existing hardware in ABM
- DMA can be used to service data transmission at the ABM to minimize CPU overhead

Disadvantages

- Requires additional hardware transceivers at device end of link
- Specialized firmware required for AMBSI
- A new interface type is added
- DMA from the MVME synchronous serial ports is not supported by VxWorks, so additional software development is required
- Not inherently multi-drop, so synchronization or concentration is required when a second down-converter is added for the production system

4.3 Use FPDP

In this design, the Front Panel Data Port (FPDP) standard would be used for the data transmission. This would reuse elements of the FPDP design planned for use in the prototype correlator. Unfortunately this hardware has not been designed yet so the reuse is purely in theory at this stage. FPDP is a 32 bit parallel data flow path that allows data to be transferred at high speeds (160 MBytes/sec.) over moderate distances (about 10 feet).

Advantages

- Reuse FPDP design from prototype correlator (except that the design does not exist yet)
- Use off-the-shelf hardware in ABM

Disadvantages

- Requires new hardware design at device end of link
- Bandwidth provided is overkill
- Price may be higher
- Length limit is exceeded if ABM is outside the receiver cabin and is close to projected separation of down-converter and ABM if ABM is inside receiver cabin
- Not inherently multi-drop, so synchronization or concentration is required when a second down-converter is added for the production system

4.4 Use Ethernet and TCP/IP

Ethernet will be provided between the ABM and at least the optical telescope and ACU subsystems. A viable option is to also transmit the total power samples over Ethernet to the ABM and thence onto the ATM link. In this scenario, additional processing power

would be required at the down-converter itself to buffer the samples sufficiently to allow them to be transferred over the non-deterministic TCP/IP channel.

Synchronization could be achieved by having the ABM tell the down-converter module (over CAN or Ethernet) that the pulse number of the *next* pulse will be a certain number (e.g. 0). When the module sends back blocks of total power values over Ethernet the pulse-number(s) can be transmitted with the block of values. In this model, the ABM performs very little processing on the data and world mainly reformat it for transmission to the central building.

Advantages

- Reuse one of the two standard networking protocols (CAN and Ethernet)
- Very little additional load on ABM
- Inherently multi-drop, so that the addition of a second down-converter for the production system is handled transparently

Disadvantages

- Requires new hardware design at device end of link
- Requires a processor to support Ethernet at the down-converter which may be undesirable for reasons of RFI

5 Chosen Design

Minimizing the number of interfaces in the system is widely agreed to be an important principle, providing of course that an existing interface can sensibly be reused. For this reason, options 4.1 and 4.4 are the most desirable solutions. Testing indicates that the interrupt loading on the MVME2700 Single Board Computer planned for the ABM is not prohibitively onerous. The Ethernet option outlined in Section 4.4 would require additional hardware and software development at the down-converter, which can be avoided in the short term by using a CAN bus and the AMBSI hardware.

Previously, the solution outlined in Section 4.2 had been proposed as a way of avoiding the interrupts loading problems. Subsequent investigations have shown that VxWorks does not support the DMA capability of serial ports 3 and 4 of the MVME 2600/2700 SBC. This introduces a potentially risky development task which it was initially assumed could be avoided. Since the interrupt load has been shown to be less of an issue, the serial transmission option has been discarded.

Given the benefits of hardware and software reuse, and the specter of looming deadlines, the proposed solution is therefore the dedicated CAN bus outlined in Section 4.1.

This option is illustrated in Figure 1. The total power data is transmitted over a dedicated CAN bus to a multi-port CAN interface on the PCI bus of the MVME 2700 ABM. These CAN ports are provided by a TEWS DatenTechnik TP816 PMC module. A VxWorks

driver has been tested for this card together with code implementing the master protocol defined in ALMA Computing Memo #7.

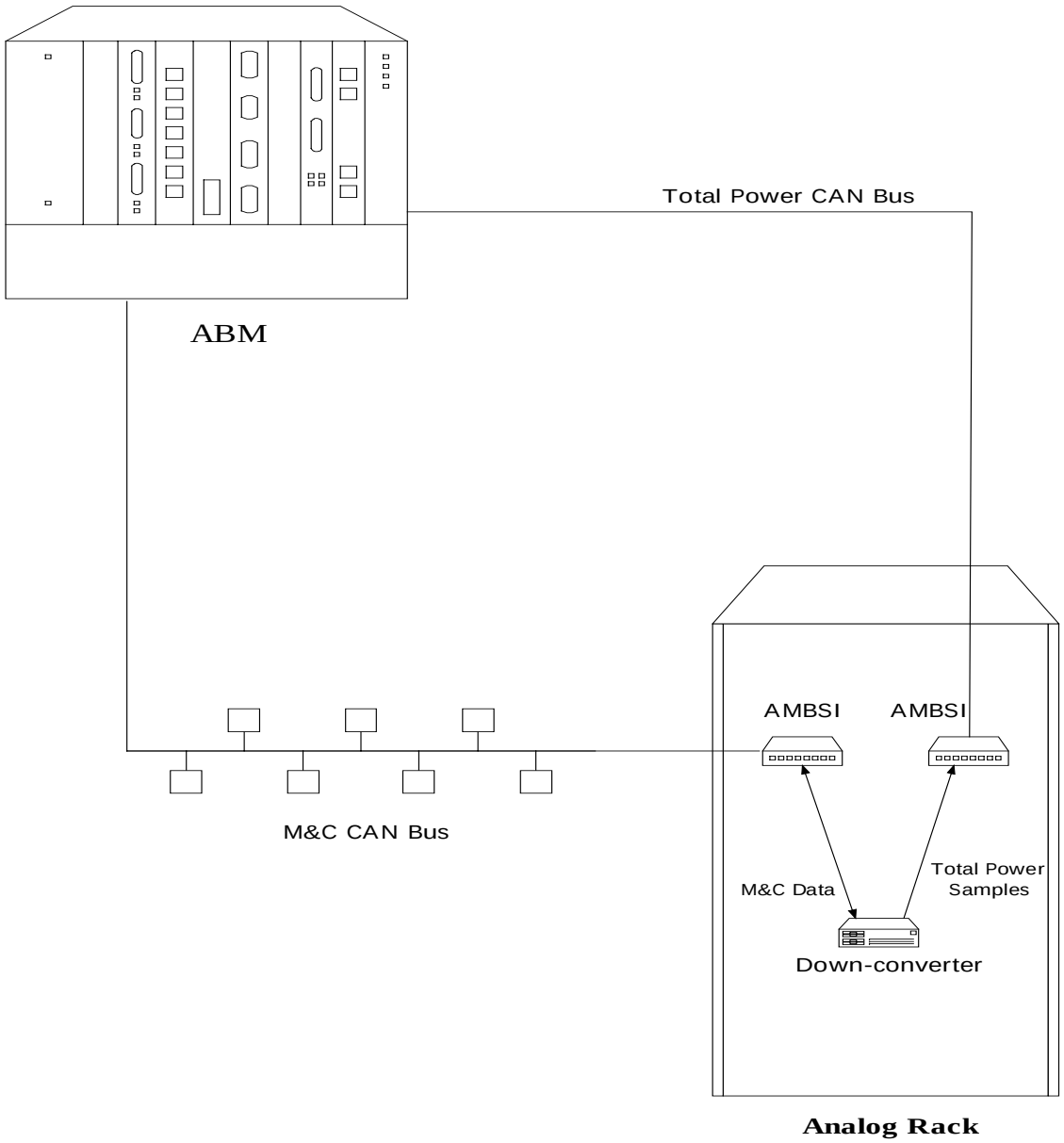

Figure 1: Option 1 Hardware and Communications

The down-converter side of the bus will be an AMBSI, with firmware to allow the total power analog-to-digital converters to be read at the precise timing instants required. The existing CAN slave code can be reused as-is. Interfacing to the A/D converters can be achieved via the SPI port of the AMBSI or the external memory bus if a parallel interface is more suitable.

Synchronization

The AMBSI collecting the total power data would sample each of the 6 A/D converters every 2 ms aligned with the 48 ms timing events. Each value would be stored in local RAM until the next timing period when they would be available for transmission to the ABM. In milliseconds 24-44 of a timing period, the ABM could solicit the samples obtained in the previous timing period. If the total power data is not currently required, the ABM will not solicit the data, with no effect on the sampling module. This scheme is illustrated in Figure 2.

Note that all the data taken during a specific 48 ms interval is transmitted during the subsequent timing period. Thus, the entire transmission needs to take much less than 48 ms. There will be 24 sampling events in every 48 ms interval, each with six 24 bit samples. Therefore, 24*6*3 = 432 bytes will need to be transmitted in a 48 ms interval. This can be mapped into 54 CAN messages, leading to 1125 CAN messages per second.

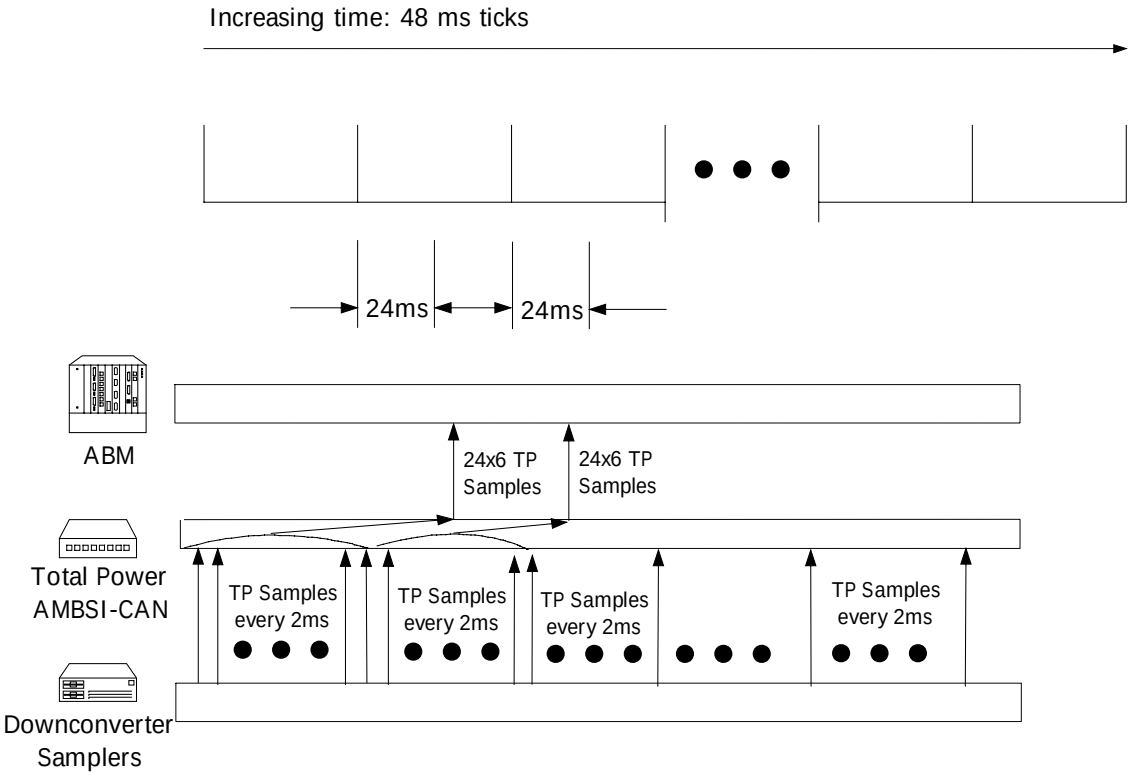

Figure 2: Possible synchronization scheme

Other Issues

Should the interrupt load of the proposed solution prove too much for the ABM to handle in conjunction with its M&C tasks, a simple solution is to add a second processor card with CAN interface solely to deal with the total power data. This would require no new hardware or software since the control system is already based on a distributed architecture. Although this is somewhat inelegant, it is anticipated that it would be an

interim solution for the Test Interferometer only, as Moore's Law should ensure that a suitably powerful processor is available for the final array.

Additional features we might need include the ability to selectively enable/disable particular total power channels. This can be achieved by the ABM only requesting the data it wants over the CAN bus. The total power data can be a useful monitor point in its own right (for example, it might be used in setting levels for the sampler). We don't need the high speed stuff all of the time so a single read should be possible as well.

The interface to the digitizers themselves is still TBD. It seems that many sigma-delta digitizer ICs of 16/22 bits have an SPI serial interface. The SPI port of the C167 would be available to provide this, although additional digital I/O bits would be required to select individual devices. If we implement the TP digitizer with a voltage to frequency converter plus counter, an intermediate micro-processor (to handle all 6 detectors/digitizers) might still be required.

Handling the two down-converters of the production system would be achieved by simply adding an additional CAN node for the second down-converter on the dedicated total power bus. Each module would be identical, with each having a different CAN node address.