Development Upgrades of the Atacama Large Millimeter/submillimeter Array (ALMA)

Study Closeout & Lessons Learned

Digital Back End Antenna Article

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1.0 Study Summary

This document will serve the purpose of the Closeout and Outcomes report for the ALMA Development Study on a Digital Back End Antenna Article. The author would like to thank Electrical Engineer Sylas Ashton, who directed and provided nearly all of the effort done in the study.

A completely digital Back End system is critical for ALMA's future and will support key growth areas as identified in the 2030 Pathways to Developing ALMA. These growth areas are: the development of a digital system that accommodates a doubling of the telescope's data rate, accepting wider Intermediate Frequencies (IFs) in Front End receivers, and possibly supporting simultaneous observing by two bands.

Two technical risks were explored in the study. First is whether existing commercially-available Analog to Digital Converters (ADCs) can provide the high-speed sampling at 24GHz as specified by the manufacturers. Secondly, Digital Signal Processing (DSP) at throughput rates higher than the Field Programmable Gate Array (FPGA) digital clock was designed and investigated.

A survey of the available ADCs led to a chosen unit and an electronics design was developed per the design summary below. The DSP was developed and successfully simulated to confirm that the overall approach would meet timing and performance requirements.

The study ran into a major issue during fabrication. The complex and expensive FPGAs used were damaged during placement due to the board's design, thickness, and material used. Efforts were made to repair and re-use the FPGAs, but they were ultimately unusable. At this stage in the project, the resources required to redesign the board and procure additional components were unavailable due to commitments in other ALMA research and with ngVLA reference design work. This led to the decision to close the study, document the designs, lessons learned, and return remaining funds.

2.0 Design Summary

2.1 Digital Back End Antenna Article

The Digital Back End Antenna Article (DBEAA) consists of three pieces of electronics – an RF clock circuit, a sideband gain equalizer circuits, and two digitizer boards. The RF clock circuit multiplies the 4GHz from the DGCK to the 24GHz clock signals required for each of the four digitizers. The sideband gain equalizer consists of an equalizer and an amplifier for each of the four sideband signals from the Front End and feeds the signals to the four digitizers. The two digitizer boards each have two ADCs, a large FPGA, 12 10Gb/s SFP+ fiber optic receivers, and a PC104 daughter board for M&C.

2.2 Clocking

The clocking for the DBEAA uses the 250MHz and the 4GHz from the DGCK. This allows the delay functions in the DGCK to be used to delay the 24GHz with minimal change in the monitor

and control. The design uses a Minicircuits RMK-2-1262 frequency tripler to go from 4GHz to 12GHz, followed by a Hittite HMC578 frequency doubler to go from 12GHz to 24GHz.

Multiplying the 4GHz clock from the DGCK module to 24GHz results in a RMS jitter of 6.5 degrees, which causes a 0.64% loss of correlation. The jitter is likely better than measured as the 1 to 10 Hz phase noise was dominated by the phase noise of the test set. The 24GHz clock had spurs at 16GHz and 20GHz that were roughly 30dBc. The 24GHz clock requires a filter between the last amplifier and the splitters in order to properly suppress the spurs.

2.3 Gain Equalizer

The HMC6545 dual gain equalizer chosen for the IF signals performs as expected as a single path device. Crosstalk between the two channels was -30dB, which is generally considered too high to use both paths. The return loss on both the input and output necessitates the use of 6dB attenuators on the input and output of the gain equalizer. The maximum gain of 12dB was insufficient to be the sole amplifier for the IF signals, and the maximum output power of 2.5dB was insufficient to be the last amplifier before the ADC. This necessitated a 20dB amplifier on the output of the gain equalizer to obtain the +3dBm output required to drive the ADCs. The range of the programmable preamp stage of the gain equalizer is 36dB, which satisfies the 13dB input range requirement of the current IFP.

2.4 Power up

The Digital Downconverter board runs on 7V and -7V. The -7V powers the ADCs and supporting electronics, while the 7V powers the FPGA, the transceivers, and the PC104. The Digital Downconverter board powers up with the regulators for the FPGA and transceivers off. The PC104 controls the power-up sequence of the FPGA through the ISA bus using the address decoding CPLD on the Digital Downconverter board. The power-up sequence has been successfully implemented and optimized to minimize inrush current.

2.5 Code

There are three pieces of code for the Digital Downconverter Board: FPGA, CPLD and PC104.

1) The FPGA code controls the ADCs and fiber transmitters, performs the digital down-conversion, formats the data, and has a monitor and control port to the CPLD.
2) The CPLD performs address decoding and voltage level translation between the PC104 ISA bus, and the FPGA. In addition, the CPLD creates a bridge between the ISA bus and the EEPROM, and provides IO to control the voltage regulator enable pins.
3) The PC104 code controls the power-up sequence, reads the EEPROM configuration data, loads the FPGA code and provides monitor and control. Since this was not the focus of the study, the design of the monitor and control borrowed heavily from the DRX M&C design used in the EVLA system.

   The PC104 successfully interfaces with the EEPROM and the CPLD control registers, and successfully provides the power-up sequence to the FPGA.

2.6 ADCs

The impedance of the RF input to each ADC was measured with a high speed Time Domain Reflectometer, and each input showed that the board and ADC RF inputs were well-matched (>20dB insertion loss).

The ADC clock was a 100ohm differential input, and the PCB had a 24GHz balun designed into it. This made it so the PCB connector was a single ended 50ohm input at frequencies above 12GHz.

The input impedance of the clock inputs were difficult to measure, since the Time Domain Reflectometer signal contains many frequencies below 12GHz, and therefore the input appeared to be an open circuit.

Driving the input with a 24GHz RF signal from a splitter allowed the use of a power meter to measure the power of the signal going into the clock input and compare it to a 50ohm termination and an open circuit. The measured power of the two measurements show that the input was within 10% of 50ohms at 24GHz.

2.7 DSP

The DSP consists of four blocks, each block consisting of a 24GHz complex Numerically Controlled Oscillator (NCO), a complex polyphase filter, a complex anti-aliasing filter, and an 8GHz complex NCO. The second NCO shifts the downconverted signal to a positive only frequency range so that the data is not aliased when converted to a real only valued signal that can be sent over the data transmission system. The NCO and filter code is parameterized and have been simulated in Verilog, and the test code has been successfully compiled. The compiled test code shows that the filters meet timing at 400MHz, which is sufficient since the code is designed to process the data in a parallel manner to handle data rates at many multiples of the DSP clock rate. This parallelization comes at the cost of increased use of DSP elements, which mandates the chosen FPGA. The successful simulation of the code was a major technical milestone for the project.

2.8 Data Transmission

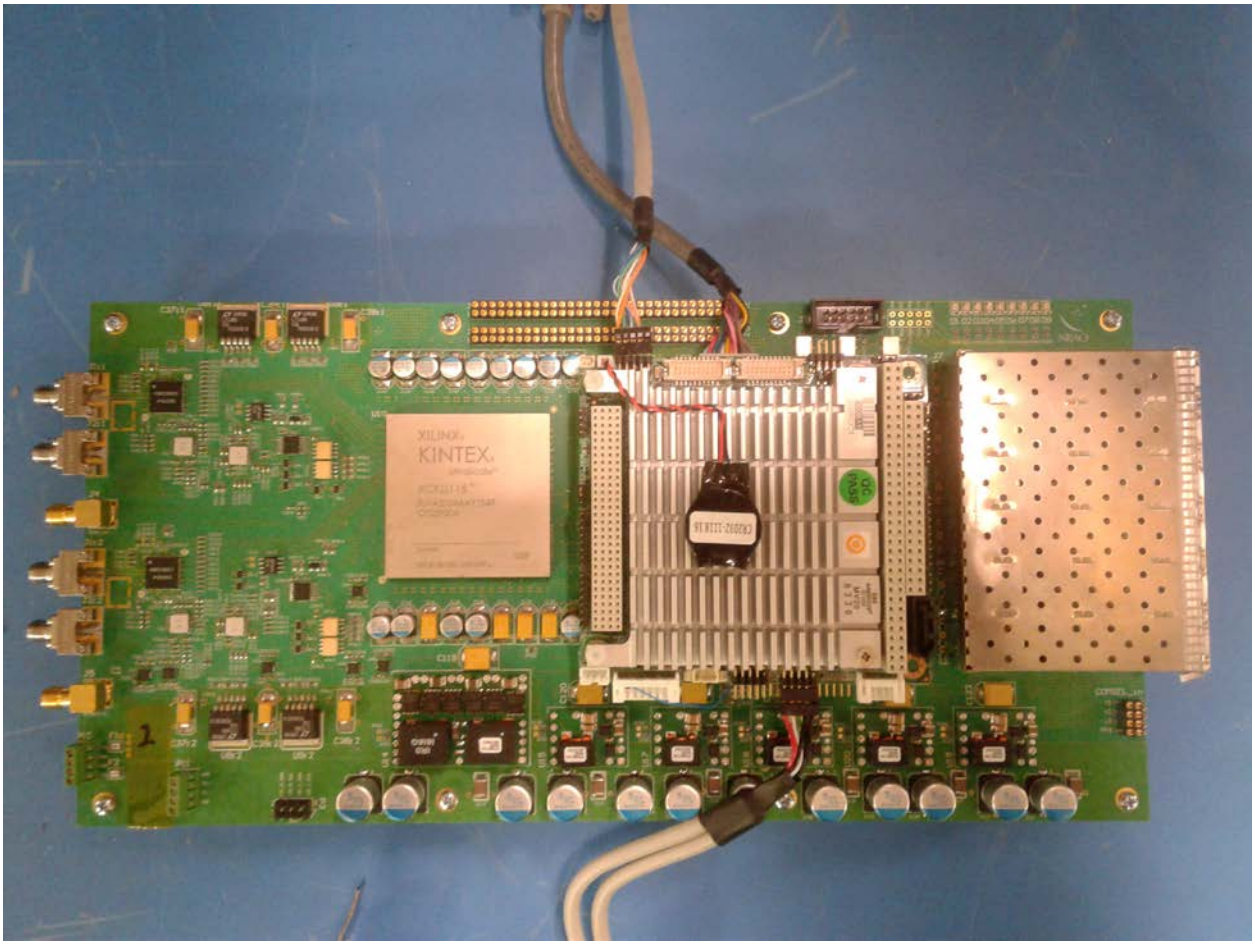
The data transmission system currently used in ALMA sends 30Gb/s over three colors for each of the four basebands, organized as one DTX per baseband. The most significant bit of the 3 bit ADCs is called the D bit, the middle bit is called the C bit and the least significant bit is called the B bit. For each DTX, the D bit of the ADCs for each polarization is multiplexed onto one color, the C bit of the two ADCs is multiplexed onto the second color and the B bit onto the third color. 20%of the data is protocol that provides data alignment and error checking.

Since the DBEAA doubles the data rate of each baseband, the protocol was modified so each color transmits one bit of a baseband without multiplexing, and the number of colors increases from 12 to 24. This is possible through the use of SFP+ transceivers developed for the telecom industry, and a housing with 12 transceivers fits comfortably on each board.

The use of the same protocol as the current ALMA system allows for the use of the current DRX modules and the DRX test sets as receivers of one board of the DBEAA.

3.0 Fabrication & Testing

The DBEAA boards were assembled by hand in stages, starting with the onboard power supplies, then the monitor and control components, and then the ADCs. The board was successfully verified that it operated as expected for each stage of assembly. The monitor and control algorithms were tested and debugged to provide the proper power up sequence to the FPGA.



At this point, the FPGA was placed on the boards with a BGA assembly machine, which unexpectedly resulted in the 1-volt power supply to be shorted on each board. Since the profile required high and prolonged heat due to the FPGA's large size and lead-free solder, the FPGA's were likely damaged by the heat during the initial placement. X-ray imaging did not show shorts under the FPGA, and thermal imaging did not show noticeable hotspots that would indicate a short in the board.

To verify the boards were not damaged, the board assembly company Process Sciences was employed to remove the FPGAs from the boards, re-ball the FPGAs with leaded solder, and place the FPGAs on unpopulated boards. The M&C and power supply components were then populated

on the new boards. Upon return of the boards, the testing results were the same, suggesting that the problem is that the FPGAs were damaged when they were initially placed.

3.1 Failure Analysis

While it is a possibility that there is a design mistake in the FPGA pin out, the odds of a single (or even multiple) mistake causing a hard short that can take more than 10 amps of current is unlikely. It is also unlikely that such a mistake could sink that much current without generating a noticeable amount of heat using a thermal camera. This pointed to a materials failure.

The top and bottom layers of the PCB were Rogers material, which does not laminate to other materials as well as FR4. The Rogers material showed signs of cracking at the corners of the PCB. While the cracking did not interfere with the performance of the PCB in this case, it does suggest that Rogers material should not be used on large boards. The combination of thermal stresses of placing the large FPGA and the Rogers material's poor lamination is expected to have been the source of the issue with the FPGA, as several of the pads for the FPGA were removed in the process of removing the FPGA from the boards. A potential replacement for Rogers material in future designs is Panasonic's Megtron 6. Megtron 6 is a high-speed, low-loss dielectric with mechanical properties similar to regular FR4.

4.0 Design Conclusions

Focusing on the design approach chosen, the following conclusions were reached.

Combining the ADC and the FPGA led to many problems ranging from layout difficulties to inflexibility of the design. While the FPGA could be reprogrammed to process data from many types of ADCs, the inability to change the 3-bit ADC became a hindrance in the design's potential use. Managing Radio Frequency Interference (RFI) seen during observations has become a significant concern in future antenna designs, which would require at least 8 bit ADCs to provide enough dynamic range.

A new design concept utilizing fiber optic transport of the high-speed data with standardized protocols, like JESD204b, between the ADC and FPGA allows for a more flexible design. This new design concept means an ADC can be placed to reduce RF circuit complexity while the FPGA itself is placed in a shielded location without degradation of performance. In addition, this new design concept will allow different ADCs to be used with the same processor, and different processors to be used with a particular ADC. This flexibility creates a modular design that allows for a simple upgrade of the design in the future.

5.0 Future Considerations

Over the course of this development study, two additional approaches for sampling broadband analog RF signals have been identified and investigated by colleagues within ALMA and NRAO.

ALMA Digital Front End Workgroup Developments

The ALMA Digital Front End Workgroup, which formed after the beginning of the DBEAA study, has concluded that separating the high speed ADC and the processing FPGA provides a more flexible system than the DBEAA. The processing FPGA and ADC are connected through fiber, and each can be upgraded independently from the other. The optical outputs from ADCs attached to different front end cartridges can be combined with an optical multiplexer to the input of a processing FPGA board, with only the lasers of the ADC for the active cartridge turned on. In addition, ADCs with 8 effective number of bits are preferred to provide the gain equalization, digital sideband separation and adaptive filtering is that is expected to be needed prior to re-quantization to 4 bits. Details are found in the documentation currently being produced by the ALMA Digital Frond-End Configuration Study.

ngVLA Developments

The ngVLA conceptual design that incorporates a similar subsystem of antenna electronics is based on the Integrated Receiver Concept described in detail in ngVLA Memo #29. The design also embraces the idea of having ADCs separated from the FPGA, in this case by a fiber optic link. The fiber link goes through an optical multiplexer, with a ADCs at each front end receiver feeding the optical multiplexer. The ADC on the receiver in use would have its lasers turned on, and the remaining ADCs turned off, providing optical selection of the receiver signals post ADC. In addition, the use of 8 bit ADCs is preferred in the lower bands for the harmful RFI expected from future wireless technology trends.

6.0 Design Archive and Hardware Storage

The design documentation, simulation results, firmware, component datasheets and all other design information are archived within a repository located at:

\\filehost\evla\techdocs\ALMA_Development_Study\Digital_Back_End_Antenna_Article\Development Files

The development platform has been placed into storage at the NRAO offices located in Socorro, New Mexico. It has been labeled in order to identify it with this study and is placed under the care of Electrical Engineer Sylas Ashton.