# Spectral Resolution and Bandwidth Upgrade of the ALMA Correlator
# Final Report Executive Summary

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# Change Record

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| A02 | 2017-01-24 | All | -- | Change focus to executive summary |
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| A04 | 2017-01-24 | All | -- | Add programmatic content, summary of software reports and ASIC evaluation report |
| A05 | 2017-02-28 | All | -- | Incorporate comments from Webber, Saez, Baudry and Escoffier |
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# 1 Introduction

## 1.1 Purpose

This is the final report for ALMA Study Project PMD-365, Spectral Resolution and Bandwidth Upgrade of the ALMA Correlator. It takes the form of an executive summary because of the large amount of data generated by this project. Additional documentation is included in separate files. All files are submitted in a zip package.

## 1.2 Scope

Programmatic information related to this project is included in this report. The bulk of the report focuses on providing an executive summary of materials used to obtain detailed cost, schedule and resource estimates for an upgrade to the ALMA 64-Antenna correlator. This includes

- System-level specifications for the upgraded correlator system
- Detailed schematics and block diagrams which serve as a basis for board costs
- Detailed design and simulation of the ASIC required for the upgrade which serves as a basis for budgetary estimates from ASIC vendors
- An analysis by an outside expert of the ASIC budgetary estimates
- Analyses, by a DSP expert, of signal processing efficiency losses
- Test and implementation plans
- Safety and product assurance plans
- Signal processing efficiency analyses
- A report on tests of a new high-speed interface to the Correlator Data Processor computers
- Reports on bandwidth tests of infrastructure in the current ALMA correlator
- Reports on recommended changes to the ALMA system to complement the correlator upgrade

Not included are cost estimates for the design and implementation of a Digital Transmission System, Receiver Board and a Tunable Filter Board, which, although housed in the correlator racks, would be provided by a separate project.

## 1.3 Applicable documents

Documents listed in Table 1 are part of this document to the extent specified herein. If not explicitly stated otherwise, the latest issue of the document is valid.

**Table 1: Applicable Document List**

| Reference | Document Title | ALMA Doc. Number |
|---|---|---|
| AD-01 | NA ALMA Development - Cycle 5 Project Proposals Web Page | https://science.nrao.edu/facilities/alma/alma-develop-old-022217/call-for-proposals-projects |

## 1.4 Reference documents

Table 2 below is the reference document list containing additional information.

**Table 2: Reference Document List**

| Reference | Document Title | Doc. Number |
|---|---|---|
| RD-01 | Document Number Assignments for Project PMD-365 | PMD-365-002-A-LIS |
| RD-02 | A Road Map for Developing ALMA<br>ASAC Recommendations for ALMA 2030 | https://science.nrao.edu/.../alma/alma-develop/RoadmapforDevelopingALMA.pdf |

## 1.5 Acronyms

A list of the acronyms used in this document is given below.

| | |
|---|---|
| **ALMA** | Atacama Large Millimeter Array |
| **AOS** | Array Operation Site (of the ALMA Observatory) |
| **ASIC** | Application-Specific Integrated Circuit |
| **BOM** | Bill of Materials |
| **CAN** | Controller Area Network |
| **CDP** | Correlator Data Processor |
| **CPLD** | Complex Programmable Logic Device |
| **DPI** | Data Port Interface |
| **DRX** | Data Receiver (part of DTS below) |
| **DTS** | Data Transmission System |
| **EDM** | Electronic Documentation Management (SiteScape Web system) |
| **FA** | Final Adder |
| **FPGA** | Field-programmable Gate Array |
| **HVAC** | Heating Ventilation and Air Conditioning |
| **ICD** | Interface Control Document |
| **IF** | Intermediate Frequency |
| **IPT** | Integrated Product Team |
| **LTA** | Long Term Accumulator |
| **LRU** | Line Replaceable Unit |
| **NRAO** | National Radio Astronomy Observatory |
| **OSF** | Operations Support Facility (of the ALMA Observatory) |
| **PCB** | Printed Circuit Board |
| **PLL** | Phase Locked Loop |
| **QCC** | Quadrant Control Card |
| **SFP** | Small Form-Factor Pluggable; industry standard transceiver |
| **SFP+** | Enhanced SFP; transceiver capable of data rates to 16 Giga-bits/sec |
| **TE** | Timing Event |
| **TFB** | Tunable Filter Board |
| **VHDL** | VHSIC Hardware Description Language |
| **VHSIC** | Very High Speed Integrated Circuit |

# 2 Introduction

The abstract for the Study Plan of this project states "The plan is to study the means, integration consequences, cost, and labor requirements for increasing the spectral resolution of the 64-antenna ALMA correlator by a factor of 8. We also plan to study how this can be an initial step towards doubling the bandwidth of the correlator." Considering this, the project has over-delivered: the study project resulted in a detailed plan for both a resolution and a bandwidth increase to the existing ALMA correlator. The clear evidence for this is that our team submitted a development proposal on January 30, 2017 with a thorough plan for increasing the resolution of the existing correlator by a factor of eight and the bandwidth by a factor of two. We increased the scope of our study because ALMA scientists appeared to be much more interested in a bandwidth increase than a resolution increase.

Details of how this was accomplished can be found in this report. In general, the approach was first to complete a design for the upgrade, from the top level to the component level and then send the designs to industry for budgetary estimates. Schedules and labor estimates were based on experience with the design, test and installation of the current ALMA correlator. In addition, analyses and simulations were carried out to verify that the design was sound.

The next section of this report concentrates on programmatics (schedule, budget, scope of accomplishments) while the following sections provide a summary of the detailed documentation that was generated to meet the goals of the project. In short, the goals of the project were met within the allotted schedule and budget. Additional scope is planned with remaining funds. Some risks were identified and we will attempt to reduce these in the coming months.

# 3 Summary of Programmatics

## 3.1 Management of Schedule, Budget and Scope

Most of the items listed in the original schedule were completed. One board design was completed only to the block diagram level, not to the schematic level. However, this was not an impediment to completing the main goal of the project: to provide a cost and schedule estimate for upgrading the ALMA correlator. From the block diagram, it was clear that the board with an incomplete design was similar enough to another board design that its cost could be estimated.

Some items that were not on the original were completed as well. These include rigorous analyses of the signal processing efficiency of the new design.

Originally, we had planned to deliver one or two reports on the feasibility of software correlators. We hypothesized that these could replace a custom-hardware based correlator in 10 to 15 years. However, the volunteer labor we counted on for this sub-project (an engineer at NVIDIA and an NRAO scientist who was transitioning to VLBA director) did not materialize. The report by the parallel, SAO-led correlator study project addresses this topic to some extent and suggests that hybrid technology solutions, involving FPGAs, ASICs, GPUs and CPUs, should be carefully considered.

The project was completed under budget. There are two main reasons for this. First, some of the required equipment did not have to be bought; unused, locally available equipment was used instead. Second, some of the collaborators were not able to provide the amount of work to which they had committed. In some cases, this was picked up by in-kind labor, which was not charged to the project. In other cases, the proposed work was completed faster than scheduled.

The scope of the project was completed. With left-over funds, additional scope will be provided during the coming 4 months.

### 3.2 Loose Ends

During the course of the project, it became clear that there is risk in transmitting data at twice the current rate through cables in the existing correlator. The risk was mitigated to some extent by bench tests. However, the 64-Antenna Correlator is a much noisier environment than a bench, so this did not mitigate all of the risk. Part of the additional scope mentioned above addresses this risk. Our plan is to fabricate a subset of the driver and receiver boards for the cables and test them in-situ in the correlator in Chile during down-time this summer.

### 3.3 Lessons Learned

A concern, early on in the project, was that a team-member who was working at a 20% FTE rate would have insufficient time to complete his assigned tasks. However, this team member worked very efficiently and, in fact, completed additional tasks. This result provides confidence that we can use certain part-time employees in a development project, should it be funded.

The fact that the due date for the ALMA development proposal was 1 month prior to the end of this study project was not optimal. Some rearrangement of priorities was required to get the development proposal in on time.

### 3.4 Follow-on Efforts

One follow-on effort is described in Section 3.2 above. In addition, our plan is to be ready for production should the correlator upgrade development project be funded. To accomplish this, additional work will be carried out during 2017, funded from other sources. In particular, the ASIC design will be simulated in an FPGA, personalities for the various FPGAs in the system will be designed, the detailed design of the Final Adder will be completed and CDRs for the board designs will be completed. See Section 7 for more detail.

## 4 Correlator Upgrade Technical Overview

### 4.1 Introduction

An important goal of the upgrade is to re-use as much of the existing infrastructure as possible to provide a minimum-cost approach in hardware and labor for implementation of the upgrade. "Existing infrastructure" includes significant parts of the existing hardware and software as well as site resources (building, HVAC, etc.). This does not mean that very little work is required, but that, compared to a complete system redesign, the costs are low.

To obtain accurate cost and schedule estimates, the study team completed detailed designs. These were submitted to industry for budgetary estimates. The study team, including an outside expert, analyzed the estimates. In addition, the study team produced a reliable assembly, test and implementation schedule based primarily on experience gained in the design, test and installation of the current ALMA correlator.

The study team also did a lot of background work so that it would be prepared to go into production immediately after the project is funded. This work includes:

- Design and test of a system to test an 8-fold increase of data to the Correlator Data Processor computers
- Tests of parts of the existing infrastructure at double the current data rate
- Analysis of signal processing losses throughout the system
- Analysis of the ASIC proposals

- Analyses of changes required by the ALMA system to support the upgrade
- High-level upgrade system specifications
- Plans for production, test, product assurance and safety compliance
- Simulation of the ASIC design

The sections below present summaries of these results. They start at the system level and continue through the sub-system and component level. The final section of the report briefly mentions additional work required so that the design is be ready for production.

### 4.2 Summary of Documentation Produced by the Study Project

To allow for easy cross-referencing of documents, the study project team devised a simple document numbering convention. This convention, along with a list of documents produced by the project, is provided in RD-01. The file is included in the zip archive and is named PMD-365-002-REP_DocumentNumberAssignments.pdf.

### 4.3 ALMA Correlator Upgrade System Overview

The "ALMA2" upgrade to the 64-antenna ALMA correlator is described from the system level. An overview of the changes to the original system is presented as well as reviews of all the design work performed so far. Details of what parts of the system must be changed and what parts do not change are presented. One of the main take-aways from this report is that the changes to the existing system are fairly easy to make. All the cards in the data path change, but these are designed to be easily swapped. The CDP computers change and these are simply mounted in racks with chassis slides. The interface to the CDPs changes from a semi-custom parallel interface to an industry standard SFP+ interface, eliminating the need for the Data Port Interface modules. The infrastructure, including racks, bins, motherboards and boards bolted into the system all remain. The file name is PMD-365-003-A-PLA_SystemOverview.pdf.

### 4.4 ALMA Correlator Upgrade System Specification

System-level specifications are contained in this document. It parallels the system specification for the current correlator with an updated system block diagram and mode

tables. For almost all modes, the bandwidth is increased by a factor of two and the number of spectral points is increased by a factor of eight. Preliminary specifications for a new feature, high time resolution, are provided. The file name is PMD-365-013-A-PLA_CorrelatorUpgradeSpecification.pdf.

### 4.5 ALMA Correlator Upgrade Cost Estimate

Hardware cost, schedule and resource estimates of the "ALMA2" upgrade to the 64-antenna ALMA correlator are presented. The cost of the highest cost item, the correlator ASIC, is based on budgetary estimates from 9 potential vendors. Costs of the next most expensive item, turn-key printed circuit boards, are based on budgetary quotes as well. Hardware plus travel costs, including a 15% contingency but not NRAO common cost recovery, are $7.5M. Labor is equivalent to approximately 3.5 FTE/year for 4 years. The file name is PMD-365-037-A-REP_SystemCostEstimate.pdf.

### 4.6 Recommended System Changes

The study project team produced two reports to describe changes to the ALMA system required by the "ALMA2" upgrade. One report treats software changes. The file name is PMD-365-039-A-REP_RecommendedSoftwareChanges.pdf. The second report treats hardware changes. The file name is PMD-365-033-A-REP_RecommendedHardwareChanges.pdf. The table below, gleaned from these reports, provides a brief summary of the scope of the modifications.

**Table 3: Summary of Required Changes to ALMA to Accommodate the Correlator Upgrade**

| Impacted Element | ALMA Subsystem | Remarks |
|---|---|---|
| Receiver | Front-End | Larger instantaneous bandwidth required to take full advantage of the wider correlator bandwidth |
| Digitization & IFDC | Back-End Digitizer & IFDC | Modifications to IF required to support 4-GHz bandwidth in front of digitizers. Faster digitizers required & digitize full IF range desirable |
| DTX and fiber optic mux/demux | Data Transmission System | New DTX & DWDM required for higher data rate |
| DRX Card and TFB Card | Correlator | DRX & TFB functions in a single card desirable |
| Correlator Control Software | Software | Minimal changes |

| | | |
|---|---|---|
| Correlator Data Processor | Software | Physical interface must change to 10 GbE. Software and hardware upgrade to handle packetization and 8X higher data rate. |
| TelCal | Software | Must be modified to deal with wider IF, TFB bandwidth and VLBI compatibility |
| ALMA Observing Tool (OT) | Software | Must present new options to the users. |
| Delay Tracking | Software | The number of delay updates in the correlator increases by a factor of two. A plan to deal with this may impact systems outside of the correlator. |
| Networking Infrastructure | Software/hardware | Higher data rates, due to a larger number of spectral channels, has consequences to data transmission from CDP master to CONTROL, TELCAL, and ARCHIVE. Switching all links to a 10 GbE environment will be necessary if all correlator modes are to be enabled for science observations.<br>Spectral averaging and longer integration times might be used to limit data rates, and volume, until network and archiving infrastructures are ready. |

**Table 3. Summary of required changes to ALMA to accommodate the correlator upgrade.**

In addition, the deployment schedule must be carefully coordinated amongst all impacted groups to minimize down-time. Note also that a two-phased approach to the correlator upgrade, where resolution increase is in the first phase and bandwidth increase implemented in the second phase, may be helpful in planning the implementation. This is because the resolution increase requires no enhancements in the Front End, Back End Data Transmission and TFB sub-systems).

It must be emphasized that these documents provide only a starting point for ALMA system engineers. They are ultimately responsible for determining the full scope of system impacts.

## 4.7 250-MHz Correlator Interface Qualification

A major premise of the upgrade is that the hardware infrastructure can run twice as fast as it presently does. The study team conducted tests on several parts of the system to validate this premise. This report summarizes a series of tests that were conducted to assure that the current correlator infrastructure (racks, cables, etc.) would operate reliably at double the current system data rate.

Two primary types of data transmission paths were tested: first, data transmission between printed circuit boards (PCBs) on the same mother board, and second, data

transmission between boards connected by shielded-twisted-pair cables. Results of the tests of the motherboard paths showed that data can be reliably recovered at the faster data rate. Some additional signal processing is required to do this, but it is well within the capabilities of the FPGAs that will be used in the upgraded design. Tests of the rack-to-rack interface show that the cables perform adequately at the increased data rate. The file name is PMD-365-027-A-REP_CableInterfaceQualification.pdf. Two additional reports support this report. The first has file name PMD-365-028-A-REP_DataRateTesting.pdf. The second has file name PMD-365-029-A-REP_SITestPCB.pdf.

### 4.8 Clock Phase Drift Tests

A second area of concern with respect to doubling the clock rate in the correlator has to do with clock phase drift in the correlator racks due to room temperature variations. The acquisition of data for this report has been hampered by glitches in the ALMA logging system. Once these are fixed, the report will be completed and submitted. The file name will be PMD-365-034-A-REP_ClkPhaseDrift.pdf. The logging problem will not be completed before the due date for the report, 2017-02-28, so a report will be provided later, probably in April 2017.

### 4.9 Correlator Data Processor Tests

The Correlator Data Processor (CDP) computers receive the astronomical data from the correlator hardware. The upgraded correlator will produce data at eight times the current rate. Tests to verify that new CDP computers can process data at this rate were conducted as part of this study. Specifications were generated for a test computer, extrapolated from the existing computers. A computer meeting those specifications was bought and stress-tested with 8 times the current data rate over a new SFP+ interface. The new computers were able to process the higher data rate. A summary of the tests and their results are included in the file PMD-365-025-A-REP_CDPDesignTest.pdf.

## 4.10 Signal Processing Sensitivity Analysis

The study has produced two reports that quantitatively analyze the signal degradation that occurs in the correlator due to truncation and other approximations in the signal processing.

The first document is more general and tries to gather in a single compact source a means to quantify the sensitivity degradation produced by the digital back-end, from the input of the ADC to the output of an FXF correlator. It assumes that the signal of interest (SOI) is white Gaussian noise within the frequency band of interest. Analytical expressions, procedures, and/or IPython code examples are all presented along with quantitative results using one observing mode of the ALMA correlator as an example.

The second report is quite specific to trade-offs under consideration in the design of the upgrade. It provides quantitative results, which provide guidance in making the tradeoffs. One important take-away from these reports is that the dominant sensitivity degradation is truncation, at the sampler and at the conversion from three bits to two bits in the TFBs. There are other causes of degradation but they are relatively minor. These factors become more important with 4-bit samplers and 4-bit signal processing. The reports are in the following files:
PMD-365-036-A-REP_SensitivityDegradationAnalysis.pdf and
PMD-365-035-A-REP_SensitivityEfficiencyAnalysis.pdf.

## 4.11 Logic Card Test Plan

The test philosophy of the upgrade project is to test sub-systems prior to performing system level tests. This plan details the approach for testing each type of card. In some cases, existing custom test fixtures can be used and in others, new custom fixtures must be designed.

The file name is PMD-365-026-A-REP_CardTestingReport.pdf.

## 4.12 Production and Installation Plan

This report covers more topics than its name implies. It includes the basics of a manufacturing plan, sub-system and system test plans, and an installation plan.

The manufacturing plan is similar to that of the original correlator build:

- a vendor is contracted for ASIC design, production and test
- a vendor is contracted for printed circuit board (PCB) manufacture
- PCB tests are conducted in-house
- System integration and test are done in house.

The main departure from the original manufacturing plan is that PCB layout will be done by an outside contractor instead of in-house.

The system test plan is similar to that of the original correlator build. In general the plan is to use built-in test generators and receivers to verify the data path and correlator modes. The built-in tests will be very similar to those in the current correlator.

In addition to this, extensive tests will be conducted at the OSF using a sub-set of the correlator developed by a parallel project called the "Fifth Quadrant". This correlator will be connected to live antennas, thus allowing testing "on the sky". This will also provide a dress rehearsal for installation at the AOS.

Installation and test at the AOS should be quite straightforward. Installation is primarily a matter of installing approximately 2000 new PCBs, installing new CDPs and adding approximately 270 LVDS data cables. Testing will follow the same plan as that used at the OSF and in Charlottesville, enhanced for a 4-quadrant system. Commissioning is ALMA's responsibility with support from the correlator design team.

The file name for this report is PMD-365-038-A-REP_ProductionInstallationPlan.pdf.

### 4.13 Safety Compliance Plan

This report covers hazards associated with installation and operation of the correlator upgrade. It is very similar to the safety plan for the current correlator, analyzing the hazards and proposing mitigation strategies. If the upgrade project is funded, JAO can treat this plan as the draft safety compliance plan.

The file name for this report is PMD-365-031-A-PLA_SafetyPlan.pdf.

### 4.14 Product Assurance Plan

This report provides a plan that ensures that all deliverables achieve compliance with ALMA requirements. It covers all phases of the upgrade, from procurement to installation.

The file name for this report is PMD-365-030-A-PLA_ProductAssurancePlan.pdf.

## 5 Sub-System-Level Study Project Documentation Summary

### 5.1 Schematics, Bills of Material, Reports

In order to get accurate cost estimates for the new printed circuit boards that need to be designed for the upgrade, schematics and bills of material for a representative subset of the boards were designed and sent to vendors for budgetary estimates. Manuals were written for each design explaining the designs.

In general, the schematics are similar to those for the current correlator. The boards are of course designed to be pin compatible. Current-generation components are used; this allows doubling the processing speed. There are three significant differences from the current design. First, the Station Card data flows from “top” to “bottom” on the card. This is a result of the consolidation, by the Laboratoire d’Astrophysique de Bordeaux, Univ. Bordeaux, of the DRX and TFB functionality onto what is currently the DRX card. Second, the design for the Correlator Card includes the long-term integration functionality on the board, making the design of a separate Long Term Integrator card unnecessary. Third, the new ASIC design allows the Correlator Card functionality to be consolidated so that one new card will replace four of the original cards.

Each schematic, BOM, and manual is in a separate file. The names of the files for the various designs are summarized in Table 4 below:

| Table 4. Summary of Design documents for Printed Circuit Board Designs | | | |
|---|---|---|---|
| **Design** | **Schematic** | **BOM** | **Manual** |
| Station Card | PMD-365-004-A-SCH_SCSchematic.pdf | PMD-365-005-A-BOM_SCBOM.pdf | PMD-365-006-A-MAN_SCMan.pdf |
| Stn Interface Card | PMD-365-007-A-SCH_SISchematic.pdf | PMD-365-008-A-BOM_SIBOM.pdf | P/o Corr Intf manual below |
| Corr Intf Card | PMD-365-009-A-SCH_CISchematic.pdf | PMD-365-010-A-BOM_CIBOM.pdf | PMD-365-011-A-MAN_SICIMan.pdf |
| Corr/LTA Card | PMD-365-017-A-SCH_CCSchematic.pdf | PMD-365-018-A-BOM_CCBOM.pdf | PMD-365-021-A-MAN_CCMan.pdf |
| Mezzanine Card | PMD-365-019-A-SCH_MZSchematic.pdf | PMD-365-020-A-BOM_MZBOM.pdf | P/o CC card manual above |
| Final Adder [1] | To be completed in 2017 | To be completed in 2017 | PMD-365-024-A-REP_FAMan.pdf |

[1] The Final Adder Manual describes the design approach as opposed to the detailed design.

# 6 Component-level Study Project Documentation Summary

## 6.1 ALMA2 ASIC Block Diagram and VHDL

The ALMA2 ASIC is the "correlator chip" which is at the heart of the correlator. It is a custom integrated circuit designed specifically for this project. The design is based on the design of the ALMA1 correlator chip that was designed about 15 years ago and is used in the current correlator. Because of improvements in the semiconductor processes, the ALMA2 ASIC is 32 times denser than the ALMA1 and twice as fast. It handles twice as many antennas and produces 8 times as many lags per antenna pair as the current design in approximately the same physical area.

To avoid dealing with a 32 times increase in data rate off the chip, a memory sub-system was added to the chip design. This occupies a relatively small area on the chip. It reduces the data rate off the chip by a factor of 16. Importantly, it enables high-time-resolution correlation modes by allowing a trade-off between number of lags and time resolution. Time resolution for both auto and cross-correlation products down to 1 millisecond is possible.

The block diagram is in the file PMD-365-012-A-SCH_ASIC_Block_Diag.pdf. A description of the block diagram is included in the ASIC Simulation Report, PMD-365-014-A-REP_ASIC_Simulation.pdf

The design for the integrated circuit is described in a special hardware description language for ASIC and FPGA design, VHDL (**V**HSIC **H**ardware **D**escription **L**anguage. VHSIC is yet another acronym; stands for **V**ery **H**igh **S**peed **I**ntegrated **C**ircuit.). This is included in the archive as a zip file, PMD-365-032-A-COD_ASIC_VHDL.zip.

## 6.2 ALMA2 ASIC Simulation Report

The VHDL design language allows one to carry out detailed simulations the ASIC logic. The main purpose of this report is to provide a summary of the simulations that were carried out. Logic or "behavioral" simulations of all parts of the circuit in all operational modes were completed. A second purpose is to provide an explanation of the ALMA2 Block Diagram

This document also includes a detailed description of the ASIC block diagram.

The file name for this document is

PMD-365-014-A-REP_ASIC_DesignAndSimulation.pdf.

### 6.3 ALMA2 ASIC Proposal Evaluation Report

A key component of the ALMA2 upgrade project is the new correlator ASIC that takes advantage of advances in Moore's law to work at twice the clock frequency of the original ALMA correlator while having 32 times more logic. This report summarizes the criteria for selecting an ASIC vendor and analyzes the results of a preliminary bid.

The report summarizes the current state of the ASIC design and production industry. It states our conclusion that the best design node (feature size) for the project is 28 nano-meters. It contrasts the two main design flows, bottom-up full custom and top-down semi-custom. Because of its very regular structure, the report recommends a full-custom approach.

The file name for this document is
PMD-365-015-A-REP_ASIC_ProposalEvaluationReport.pdf.

## 7 Future Work

### 7.1 Introduction

This section details work that remains to be done in preparation for starting the upgrade project. Some of it is funded from an extension of the study project while the rest will hopefully be funded from other sources.

### 7.2 CDP Processing Extension

During the study project, it was shown that the new generation CDP computer can handle the 8-fold increase in data rate resulting from the upgrade. Additional work will be performed that will determine if another factor of two in performance can be obtained through various optimizations

### 7.3 PCB Design Finalization

During the study phase, PCB designs sufficient to obtain reliable pricing were completed. During 2017 additional work will be completed to finalize the designs so that they are ready to go to the vendors.

### 7.4 Additional ASIC Simulations

Additional simulations of the ASIC's VHDL code are planned. The behavioral simulations that were completed during the study project will be supplemented with simulations in an FPGA.

### 7.5 FPGA Design

FPGA designs required for the various new boards will be completed.

### 7.6 Verification of the FPGA Personality Storage Scheme

The size of the personalities required for the new FPGAs in the new board designs is too large to fit into the existing memories in the correlator control cards. (The control cards do not change in the upgrade.) A new system for personalities has been designed. However, the design has not been completely verified. Upgrades to system firmware and software are planned test the new personality storage scheme.

### 7.7 In-situ Data Rate Tests

To minimize risks, data rate tests in the AOS correlator are planned. These will test that the data rate between the Station Racks and Correlator Racks can be doubled. To accomplish this, the following steps will be taken:

- Complete the design of the Station Interface and Correlator Interface boards
- Contract the PCB layout and fabrication of 5 to 10 boards to a PCB vendor
- Test the operation of these boards in the 2-antenna correlator in Charlottesville
- Test the operation of these boards in the 64-Antenna correlator in Chile during down-time periods

## 7.8 Mezzanine Card Prototyping

The Mezzanine Card, which supplies power to the Correlator Card, takes a completely different design approach from the current Mezzanine Card. Instead of using pre-packaged power supply "bricks", it uses an approach with more discrete components. The approach is similar to that used in the design of the "SNAP" board by the correlator group. This saves money and adds flexibility. It also adds some risk due to the fact that it is an analog design sensitive to PCB layout. For this reason, it would be useful to try to find the time and funds to prototype and test this board during 2017.