Closeout report for

"Advanced Materials and On-wafer Chip Evaluation: 2nd Generation ALMA Superconducting Mixers"

ALMA Development Studies (Cycle 3)

Michael Cyberey
Arthur Lichtenberger
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on behalf of the University of Virignia Superconducting Device Group (UVSDG)

University of Virginia
Microfabrication Laboratory
Superconducting Device Group

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Study Plan

1.1 North America ALMA Strategic Context

ALMA's continued long-term success is of critical importance to the North America (NA) millimeter and submillimeter radio astronomy community. The eight highest ALMA bands (of ten total bands), at which the highest resolution observing is obtained, use superconducting-insulating-superconducting (SIS) based front ends. Maintaining the NA investment in Band 3 and Band 6 and creating future significant NA opportunities requires an efficient and productive access to a robust SIS foundry. Realizing a next generation of ALMA SIS mixers that operate near their quantum limit at higher frequencies (Band 8, 9, 10, 11) will require new materials and similar access to such an advanced SIS foundry. At present, there exists only one North American SIS foundry capable of making and developing such radio astronomy mixers - the University of University of Virginia Microfabrication Laboratories (UVML). The UVML has demonstrated SIS mixers that exceed the design specifications of ALMA's Band 3, 6, 7 & 8, and is the SIS foundry for all Band 3 and Band 6 SIS mixer chips.

The UVML has a long-standing internationally recognized program of excellence in THz materials, devices, circuits, and metrology. This effort began in the early 1970s with the pioneering development, in a historic collaboration with the National Radio Astronomy Observatory (NRAO), of semiconductor Schottky barrier diodes and later superconductor detectors for radio astronomy. The Superconducting Device Group at the University of

Virgina (UVSDG) at the UVML has since closely collaborated with astronomical receiver groups and the NRAO for more than 30 years to develop state of the art superconducting receivers for use on radio telescopes throughout the world. The UVSDG was the first group to develop the SIS "SOI" mixer architecture with ultra-thin Si chips and Au beam leads [1] and the first group to develop inductively coupled plasma (ICP) grown AlN tunnel barriers [2] that have led to the highest quality Nb/Al-AlN/Nb and Nb/Al-AlN/NbTiN SIS junctions. The UVSDG's SOI mixer chip architecture and AlN barrier material are ripe for ALMA's exploitation for more sensitive, wideband and sideband receivers, better performing higher frequency second-generation receivers and array receivers.

In addition to the technical progress reported in this document, the received funding is critically important for continuity of ALMA's essential infrastructure by helping to maintain the UVML, which is the sole North America SIS mixer foundry.

Study Overview

The ALMA development study contained two main thrusts. The first was a study of the suitability of an alternative materials deposition technology – Reactive Bias Target Ion Beam Deposition (RBTIBD) – that offers unique capabilities to tailor materials and interfaces. We report on the use of our existing RBTIBD tool, in a set of experiments, to study and optimize NbTiN and AlN film growth. Using the knowledge gained from these experiments, we report the first ever realization of all-NbTiN NbTiN/AlN/NbTiN SIS junctions, grown at room temperature, through direct epitaxial growth of the AlN barrier layer. The resulting junctions demonstrate excellent I-V characteristics with sum-gap voltages of 5.0 mV and $\frac{R_{sg}}{R_n}$ ratios in excess of 10.

The second thrust was the development of an all-wafer SIS device I-V electrical characteristic screening technique. We investigated and optimized the thermal design and heat management of our existing Lake Shore cryogenic probe station and stock DC probes. This

culminated in the design and fabrication of our improved cryogenic on-wafer DC probes that, for the first time, allowed the on-wafer recording of the I-V characteristics of an SIS junction, with device temperatures below 5 K using our Lake Shore cryogenic probe station.

RBTIBD Growth of AlN and NbTiN

2.1 Motivation

The heart of the ALMA is largely championed by superconducting detector technology and SIS mixer technology, in particular, is an integral part with Bands 3-10 utilizing SIS based front ends. The current state of the art approach for ALMA SIS mixer junctions is based on magnetron sputtering and the Gurvitch Al overlayer trilayer process [3]. In the Gurvitch process, an Al overlayer is deposited onto the Nb base electrode in order to subsequently grow the critical ~1 nm tunnel barrier and a top counter electrode of Nb is deposited to complete the SIS "trilayer" stack. However, it is well known that a limiting factor to using aluminum oxide tunnel barriers comes into play when higher current density SIS tunnel junctions are desired for higher-bandwidth, higher-frequency designs, as the decreasingly thin aluminum oxide barriers are eventually shown to introduce excess leakage currents due to defects and pinholes in the barrier [4]. A suitable replacement to the aluminum oxide barrier is AlN, which can be grown by ICP nitridation of Al overlayers, a process first pioneered by UVSCG at the UVML. While significant research has been performed by the UVSCG to understand and optimize ICP AlN growth (resulting in the realization of low-noise Nb/Al-AlN/Nb based SIS mixers), the use of Nb electrodes provides an upper limit to the frequency range for low-noise mixer operation. The ideal Nb/Al-oxide/Nb junction has a sum-gap frequency of ~700 GHz. However, given actual I-V characteristics with a sum-gap voltage starting well below

2.9 mV and additional zero voltage Josephson current noise, mixer performance can suffer at 650 GHz.

ALMA Band 9 (602-720 GHz) and Band 10 (787-950 GHz) currently use all Nb SIS junctions, and their performance suffers from this material choice (particularly Band 10). SIS junctions with higher energy gap electrodes can push this optimal frequency performance limit to higher frequencies. The most likely SIS material candidates for higher energy gap superconductors are NbN and NbTiN. The performance of NbN mixers has generally been reported to be limited due to surface resistance in NbN films [5, 6] and studies of NbN/Al-N/NbN trilayer for SIS mixers have generally performed poorer than anticipated; one of the primary problems being the superconductive properties, including penetration depth, and the loss of the polycrystalline NbN thin films are sensitive to their crystal properties, resulting in "drastically deteriorated mixing properties" [7]. Such all NbN mixer approaches have even resorted to a hybrid approach of incorporating NbTiN films to serve as on-chip tuning elements [7]. All NbTiN SIS mixers are therefore clearly the optimal path to pursue.

Unlike our Nb/Al-AlN/Nb trilayer technology, the Gurvitch Al overlayer method is not a desirable path with higher energy-gap superconductors such as NbN and NbTiN, as the nitrogen at the Nb(Ti)N/Al interface would form AlN, inhibiting the proximity effect, and can lower the energy-gap of the junction [8, 9, 10]. An alternative method is the direct deposition of AlN onto the base NbTiN layer. NbTiN and the Wurtzite phase of AlN have FCC and HCP crystal lattices respectively, both are very similar closed-packed lattices with the sole difference in the stacking order of the close-packed plane as shown in Figure 2.1. Our research group briefly investigated this approach through reactive magnetron sputtering of NbTiN and AlN in our room temperature trilayer deposition tool, to grow NbTiN/Al-N/NbTiN trilayer material. The resulting SIS junctions showed signs of SIS behavior, but contained high sub-gap leakage currents, and reduced energy-gap [11]. While our trilayer deposition tool can produce high quality Nb/Al-AlN/Nb and Nb/Al-AlN/NbTiN trilayer material, direct deposition of a ~1 nm thick tunnel barrier requires slow uniform epitaxial

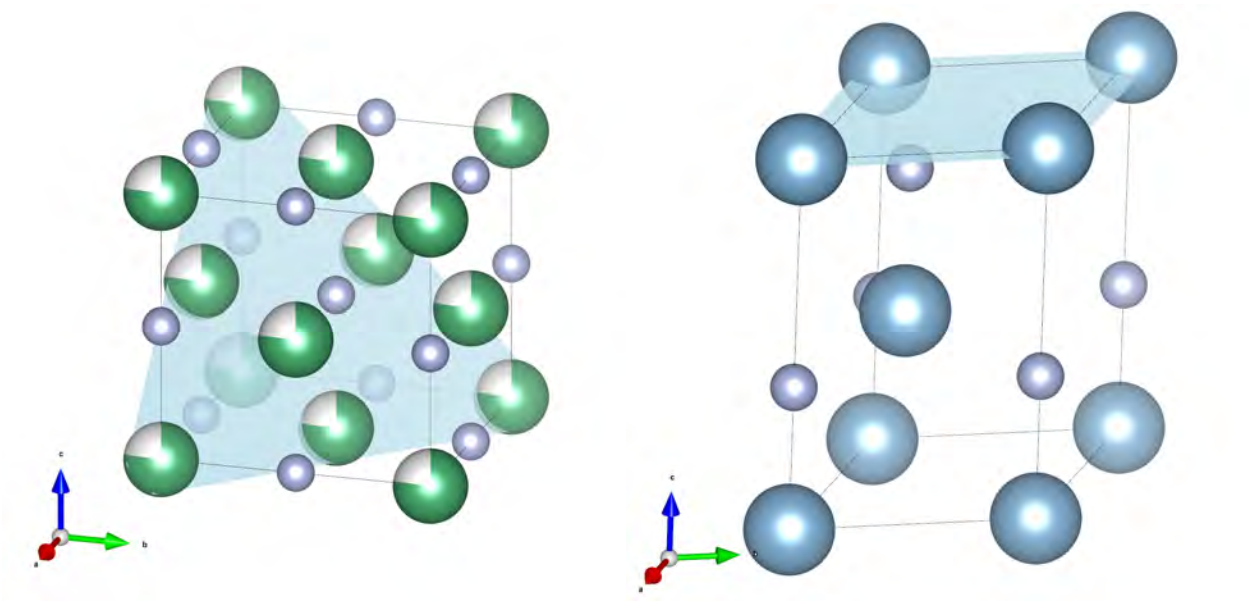

Figure 2.1: Left: FCC NbTiN with the close packed (111) plane highlighted. Right: HCP Wurtzite phase AlN with the (100) close packed plane highlighted. Both are close packed crystal structures with similar lattice constants in the close packed planes.

growth across our 51 mm substrate, and can present a challenge using room temperature magnetron sputter deposition from a 75 mm target. As part of this study, we proposed a radical departure from conventional trilayer deposition techniques, by using RBTIBD in order to realize the first ever NbTiN/AlN/NbTiN tunnel junctions with low sub-gap leakage currents and sum-gap voltages of 5.0 mV.

Our RBTIBD tool, shown in Figure 2.2, is a hybrid between ion beam and conventional sputter deposition that combines the best of each technique. The RBTIBD process utilizes a low energy broad beam ion source that reliably produces a controllable density of uniform low-energy (5-50 eV) inert gas ions that by itself will not re-sputter any surface atoms [12]. The flux and dynamics of the incoming ions to the targets are manipulated by independent pulsed DC bias supplies where the target voltage can be set while the target current is fine-tuned through the pulse width and frequency. In between the target bias pulse, the ions can also be directed at the substrate to increase energetics and ad-atom mobility, and the rotatable substrate stage is adjustable from room temperature to 650C to further control crystallinity of the deposited films. A significant advantage of this unique tool is the ability

Figure 2.2: Fig. 4. Left: Schematic of Reactive Bias Target Ion Beam Deposition system; Right: Photograph of the UVA 4-Wave RBTIBD tool that can accept up to 100 mm diameter wafers.

to precisely and separately control incoming sputtered atom energies to tailor composition, phase formation, surface roughness, and interfaces– properties critical to achieving such a direct sputtered tunnel barrier.

The first thrust of our prosed work was to ultimately realize an all-NbTiN SIS tunnel junction using RBTIBD, and our results will be presented in 3 main parts:

1: Development of high-quality closed-packed Wurtzite-phase AlN films.

2: Development of high Tc NbTiN films deposited on oxidized Si substrates.

3: Deposition, fabrication, and cryogenic testing of NbTiN/AlN/NbTiN tunnel junctions.

2.2 Development of AlN films by RBTIBD

AlN films were deposited on 51 mm diameter, 300 μm thick (100) 'bare' Si substrates with only a native oxide. The films were deposited maintaining constant pulse bias frequency, duty cycle, Ar flow and N_2 flow rates, and varying only the target bias from 500 to 900 V (the maximum bias voltage). The films were initially visually inspected for transparency and then analyzed using a J.A. Woollam Co. M-2000U® spectroscopic ellipsometer from 235-1000 nm. We chose a bare (100) Si substrate substrate as a starting point because it is

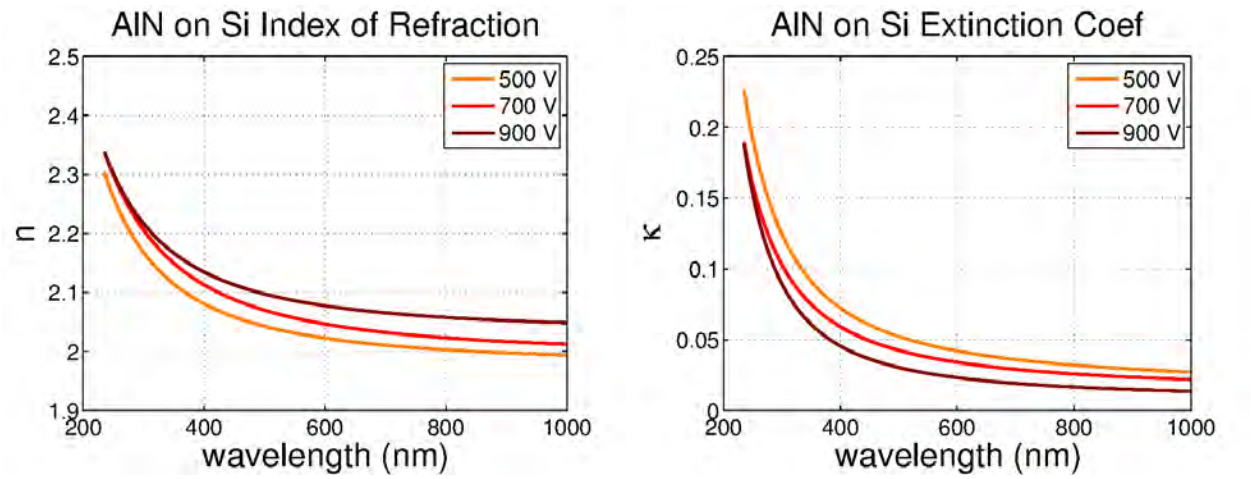

Figure 2.3: Index of refraction (left) and extinction coefficient (right) of RBTIBD AlN films determined by fitting to a Cauchy-Urbach dispersion.

an optically well-defined substrate and allowed the use of a single Cauchy-Urbach dispersion layer in our spectroscopic ellipsometry model to determine the optical constants of our AlN films. Figure 2.3 shows the index of refraction and extinction coefficient, determined by fitting to our model using J.A. Woollam CompleteEASE analysis software. For all three films, the index of refraction is within the expected values for AlN, and agrees with our previously developed model for in-situ monitoring ICP AlN growth [13]. The extinction coefficient is an indicator of dielectric loss and decreases with with increasing applied bias voltage- noting this, we fixed the voltage at 900 V, where it is lowest, for future depositions.

2.2.1 Spectroscopic Ellipsometric Analysis and Effects of N_2 Flow

After the single-layer spectroscopic model of our AlN film was developed, additional AlN samples were deposited on thermally oxidized 51 mm diameter, 500 μm thick silicon wafers, the typical substrates used for our SIS test-junction fabrication. All parameters of the RBTIBD, except nitrogen flow rate, were held constant for each run to observe the effects of nitrogen flow rate as it was varied from 1 to 20 SCCM. Film stress was measured using the wafer deflection technique with a Frontier Semiconductor FSM 128 Stress Measurement System. The deposition rate and film stress, as a function of nitrogen flow is shown in

Figure 2.4. For higher nitrogen flow rate, we see an expected and well-behaved decrease in deposition rate. However, the film stress is about an order of magnitude higher than our magnetron sputtered films, and is little affected through varying the N_2 flow rate. The exact source of the high stress observed in RBTIBD is not completely understood at the time of writing, but more information about potential ways to lower the film stress in the BTIBD tool is discussed at the end of this section.

All samples were analyzed by our M-2000U ellipsometer, and a model was built for the $Si/SiO_2/AlN$ materials stack, visually depicted in Figure 2.5. The model consists of an SiO_2 film on top of an infinitely thick Si substrate. The AlN film is again modeled as a Cauchy-Urbach dispersion on top of the SiO_2 film. However, for this particular model, we take into account the surface roughness of our AlN film through the use of a Bruggeman Effective Medium Approximation (EMA), which mixes the optical constants of our AlN film and vacuum, assuming 50% AlN inclusion. To first order, the thickness of the EMA layer is an indication of relative surface roughness among the films. Three of the samples were analyzed using AFM to calculate the RMS roughness, this is plotted alongside the determined EMA thickness in Figure 2.5. More data need be taken, but the general trend observed in Figure 2.5 indicates that the EMA layer can be used as a quick analysis for relative surface roughness among samples. The index of refraction and extinction coefficient, calculated at 650 nm from our ellipsometric model is plotted in Figure 2.5. The index of refraction is in the range expected for AlN films, and a general trend toward lower extinction coefficients at lower N_2 flow rates is observed.

2.2.2 XRD Analysis

XRD analysis of our AlN films was performed using a Rigaku SmartLab® X-ray diffraction system using Cu K-alpha radiation to verify the formation of the close-packed Wurtzite phase AlN and determine the lattice constants of our films. Figure 2.6 shows the XRD spectra of the AlN films deposited with varying nitrogen flow rates; we note the sample deposited at a flow

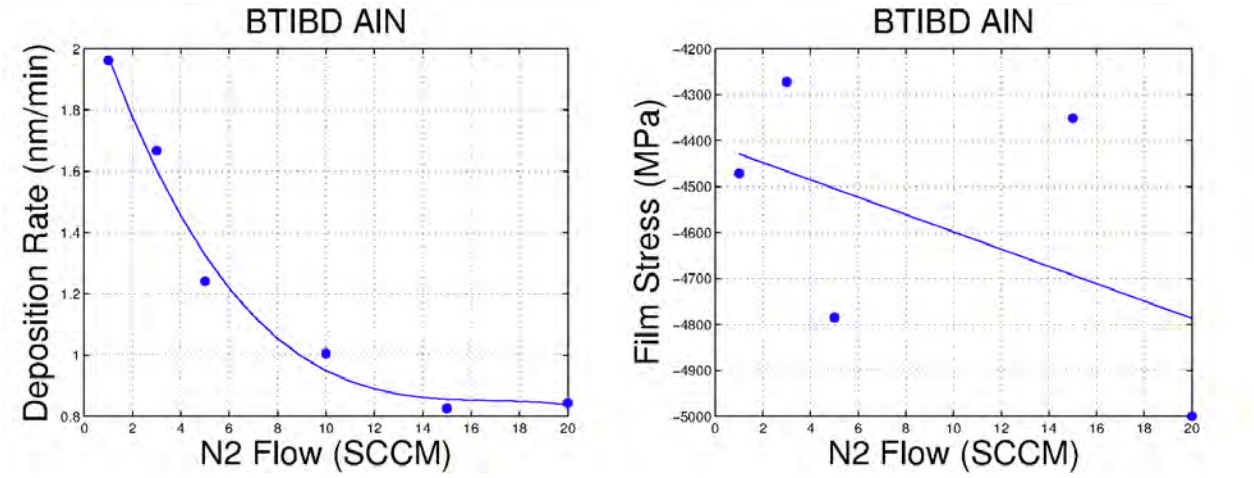

Figure 2.4: Effect of nitrogen flow on the deposition rate (left) and film stress (right) of RBTIBD AlN films deposited on oxidized silicon wafers.

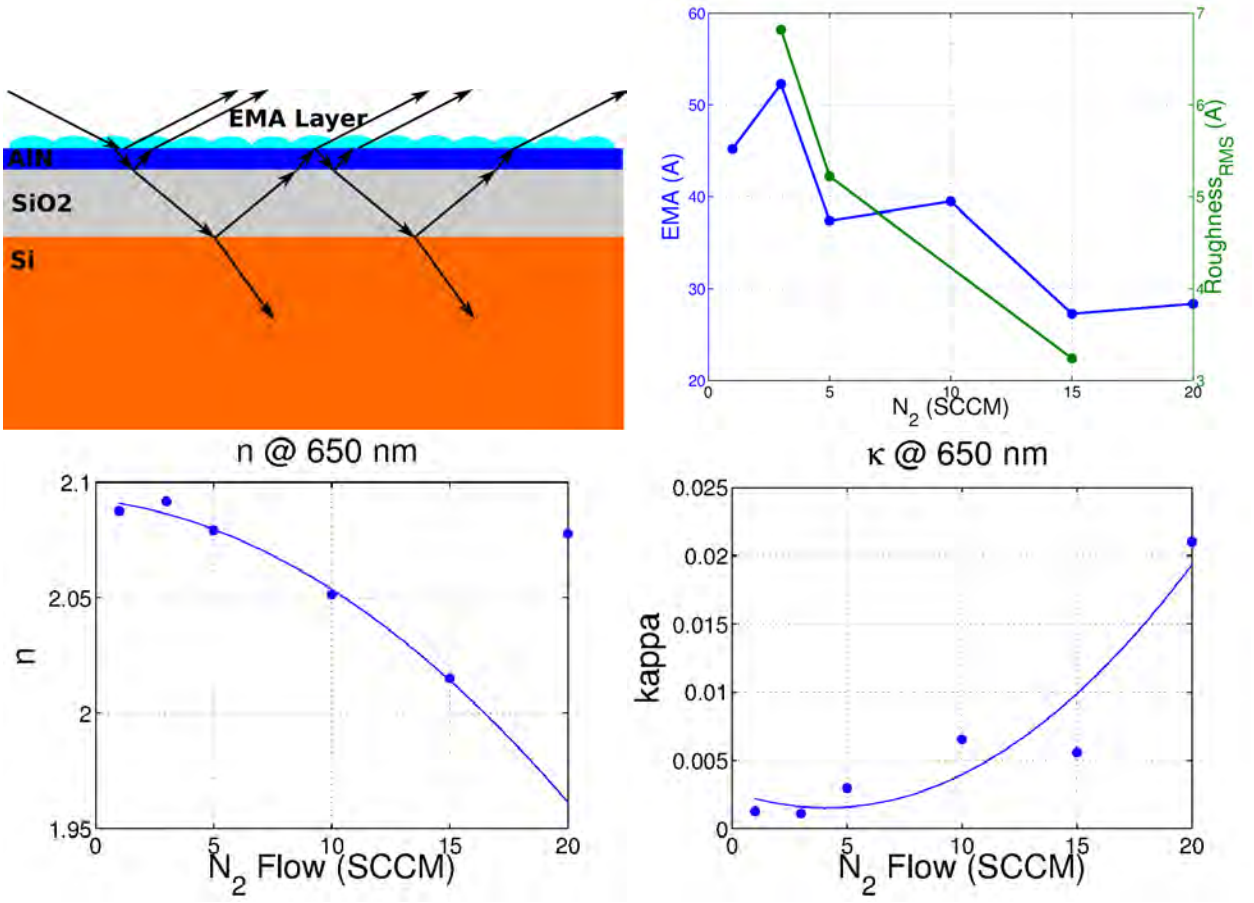

Figure 2.5: Top Left: Visual depiction of our 3-layer spectroscopic ellipsometric model, using a EMA layer to approximate surface roughness. Top Right: EMA thickness as a function of N_2 flow rate, plotted alongside RMS surface roughness determined through AFM. Bottom: Refractive index (left) and extinction coefficient (right) as a function of N_2 flow rate.

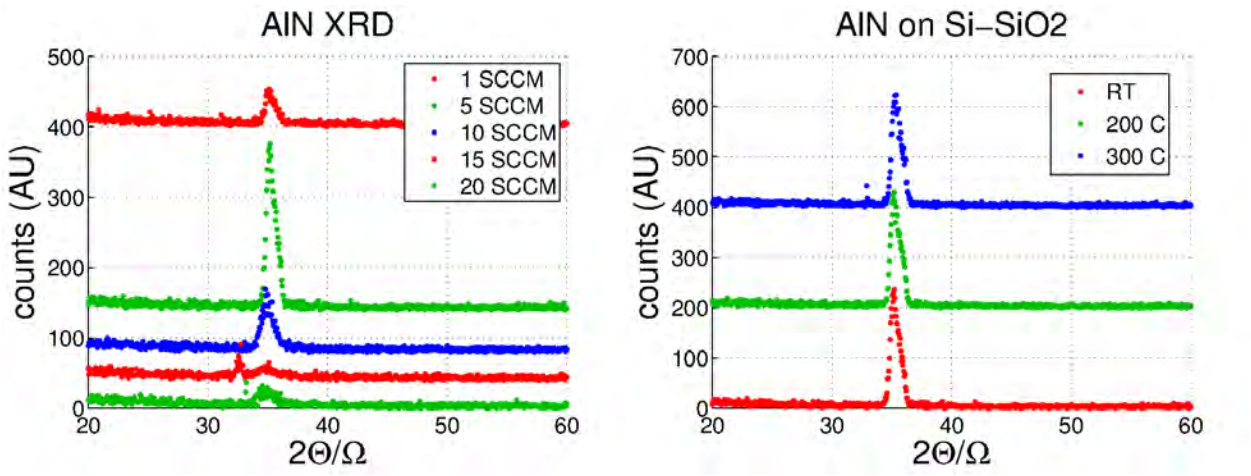

Figure 2.6: XRD 2 theta/omega spectrum, offset for visual inspection, of RBTIBD AlN films as a function of N_2 flow rate (left) and substrate temperature (right).

rate of 3 SCCM was damaged and shattered before we were able to perform XRD analysis and is omitted. The diffraction peaks observed around 35 degrees correspond to the (200) plane of Wurtzite phase AlN, and interestingly are most intense for the sample deposited with a flow rate of 5 SCCM. The $\frac{N_2}{Ar}$ flow ratio at this point is only 6.25%; previous reports of reactive DC magnetron sputtering of AlN from an Al target reported that maximum crystallinity, observed through the (200) diffraction peak, was observed with a $\frac{N_2}{Ar}$ flow ratio of 35%, a striking difference to RBTIBD [14]. The lattice constant for this film, calculated from the (200) diffraction peak, is 0.509 nm, in very good agreement with the literature [14, 15, 16]. While maintaining a fixed flow rate of 5 SCCM, 2 additional samples were deposited at elevated substrate temperatures of 200 and 300 C, to investigate if any increase in crystallinity is observed. Figure 2.6 shows the resulting 2 theta/omega spectra and we note no increase in the intensity of the (200) peak is observed. For future work, additional samples will be deposited at elevated substrate temperatures, but in the scope of this initial study, we first maintain our focus on room temperature depositions.

2.3 Development of NbTiN films by RBTIBD

An AlN RBTIBD process was developed, producing close-packed Wurtzite phase films with a lattice constant consistent with what is reported in the literature. We report the development of a RBTIBD process for the growth of higher energy gap NbTiN, for the ultimate realization of NbTiN/AlN/NbTiN trilayer. The UVSDG has vast experience with the deposition of NbTiN films through reactive magnetron sputtering of a NbTi target at room temperature. In order to maximize the energy gap of reactive magnetron sputtered NbTiN films, the $\frac{N_2}{Ar}$ flow ratio is varied until a maximum value of T_c is achieved. However, the plasma confinement inherent to magnetron sputtering causes non-uniform wear of the target, and the optimal $\frac{N_2}{Ar}$ flow ratio changes over the life of the target. For this reason, the 'voltage elevation' method is employed; using this method, nitrogen is slowly introduced to the deposition chamber after an Ar plasma is formed until the cathode voltage of the sputter gun increases to a set value. Interestingly it was found that maintaining a constant voltage elevation yields consistent NbTiN film properties over the life of the target compared to maintaining a constant $\frac{N_2}{Ar}$ flow ratio [2, 17].

However, the heart of RBTIBD tool is the low energy broad beam ion source that generates a plasma independent of the target bias. With no self-bias of the target, a different approach must be taken to optimize the amount of nitrogen to add for reactive NbTiN growth. Unlike magnetron sputtering, there are no magnets to confine the plasma above the target in RBTIBD, and the broad ion beam uniformly erodes the target. Noting this, we expect the optimized sputtering conditions to remain nearly constant over the life of the target, and for our initial study, maintain a constant optimized $\frac{N_2}{Ar}$ flow ratio.

2.3.1 Effects of Nitrogen Flow on NbTiN Film Properties

A 100 mm diameter, 6.35 mm thick NbTi (78:22 wt%, 99.75% purity) target was installed in the RBTIBD system. We used the same plasma source and target bias conditions from

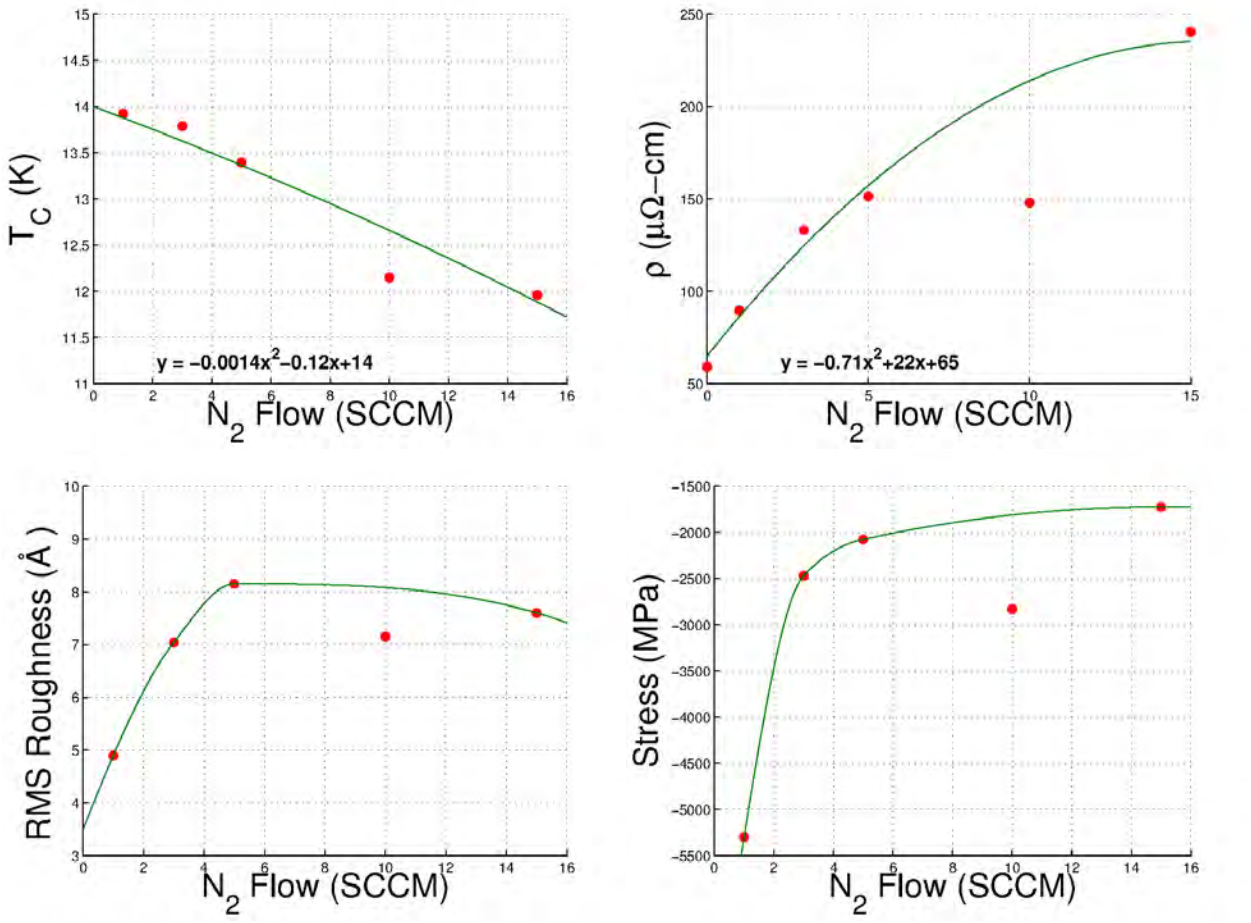

Figure 2.7: T_c(top left), resistitivy (top right), RMS surface roughness (bottom left), and film stress (bottom right) as a function of N_2 gas flow rate.

our AlN process as a starting point. The total Ar flow was maintained at 80 SCCM, and the nitrogen flow was varied from 1 to 15 SCCM. Figure 2.7 shows the measured transition temperature, resistivity, RMS surface roughness, and film stress of the resulting NbTiN films. Resistivity and surface roughness decrease with decreasing nitrogen flow to values notably lower than that of our room temperature magnetron sputtered films that have typical values of >120 $\mu\Omega$-cm and >10 Å respectively. However, the RBTIBD NbTiN film stress is notably higher, and has a sharp increase when the nitrogen flow rate is reduced below 3 SCCM.

In attempts to reduce film stress, additional samples were deposited at 1 SCCM flow rate varying the target bias from 500 to 900 V, reducing the pulse width, and installing a physical 'beam blocker' to block ions from the plasma source from reaching the sample during the

off-cycle of the pulse bias. For all cases the compressive film stress remained over 3500 MPa, and T_c was reduced.

While the best NbTiN film, in terms of smoothness, transition temperature, and resistivity occurs at 1 SCCM flow rate, the compressive film stress is remarkably high at over 5000 MPa. Taking into account the possibility of film stress relief through buckling and delamination during processing, we settled on a constant nitrogen flow rate of 3 SCCM for subsequent room temperature trilayer depositions. While these conditions didn't produce the highest transition temperature, the compressive film stress is a relatively more modest 2500 MPa.

2.3.2 Effects of Subtrate Temperature on NbTiN Film Properties

Additional NbTiN samples were deposited on oxidized Si wafers, as well as C-cut single crystal sapphire, at elevated substrate temperatures up to 575 C. The effects on resistivity, transition temperature, and film stress are shown in Figure 2.8. At increased substrate temperatures, increased transition temperature and reduced resistivity is observed, producing the highest Tc NbTiN films from the UVML to date. We found a decrease in film quality past 500 C, though we note that the vacuum feed-through started to fail at this temperature, producing a vacuum leak. Impurities in the NbTiN film are a likely cause of transition temperature reduction and increased resistivity. Most notably shown in Figure 2.8, the compressive film stress was observed to decrease with increasing substrate temperature, achieving a film stress below 1000 MPa for films deposited above 400 C. A modest increase in film quality was observed for films deposited on sapphire substrates and can be potentially attributed to the latticed matched close-packed C-plane orientation of the substrate. While sapphire substrates are not compatible with current SIS mixer designs, if increased film quality is observed due to the lattice matching of the substrate to the NbTiN film, it may open the possibility for the use of thin buffer underlayers on the SOI substrates we use in SIS mixer fabrication.

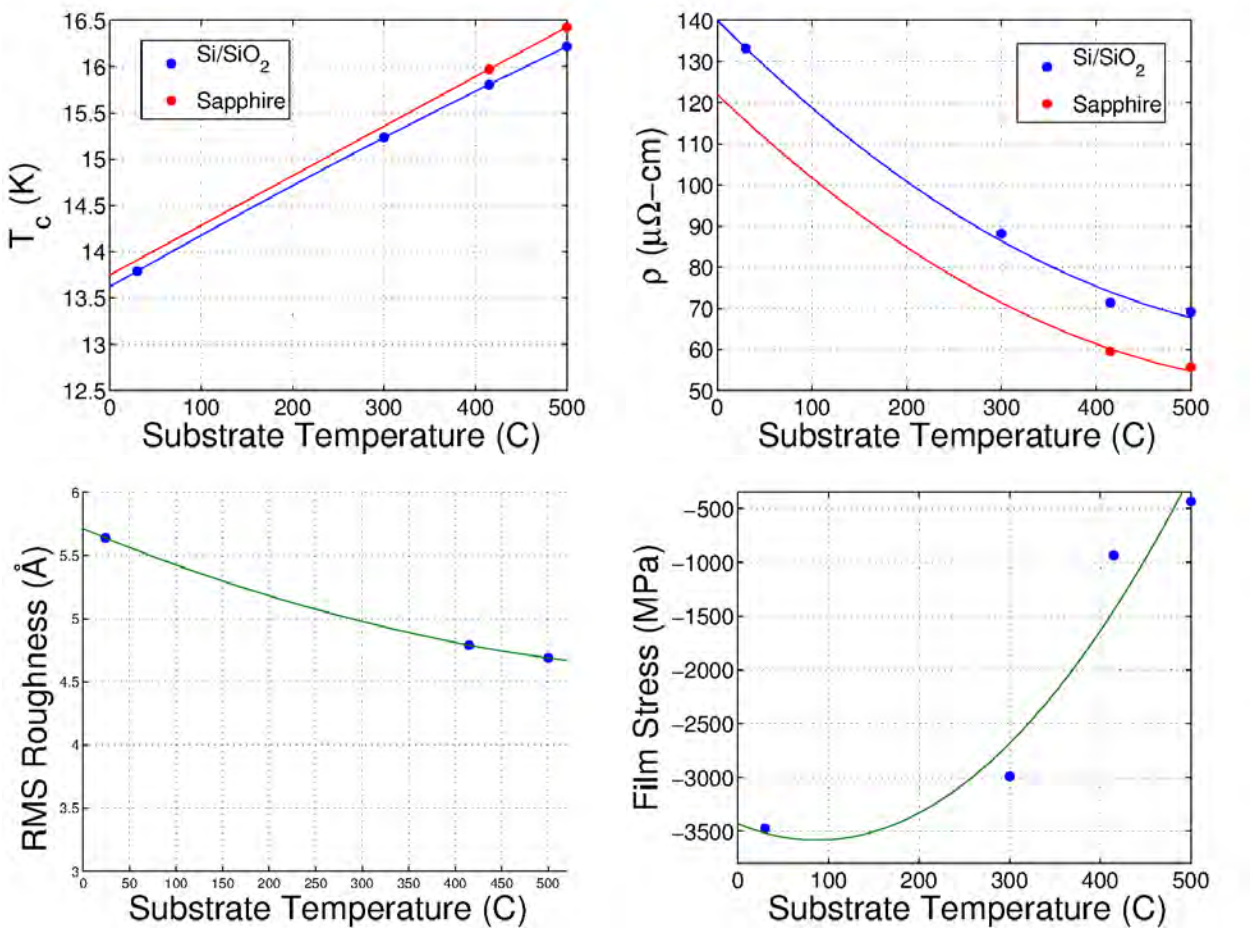

Figure 2.8: T_c (top left), resistivity (top right), RMS surface roughness (bottom left), and film stress (bottom right) of RBTIBD NbTiN films as a function of substrate temperature.

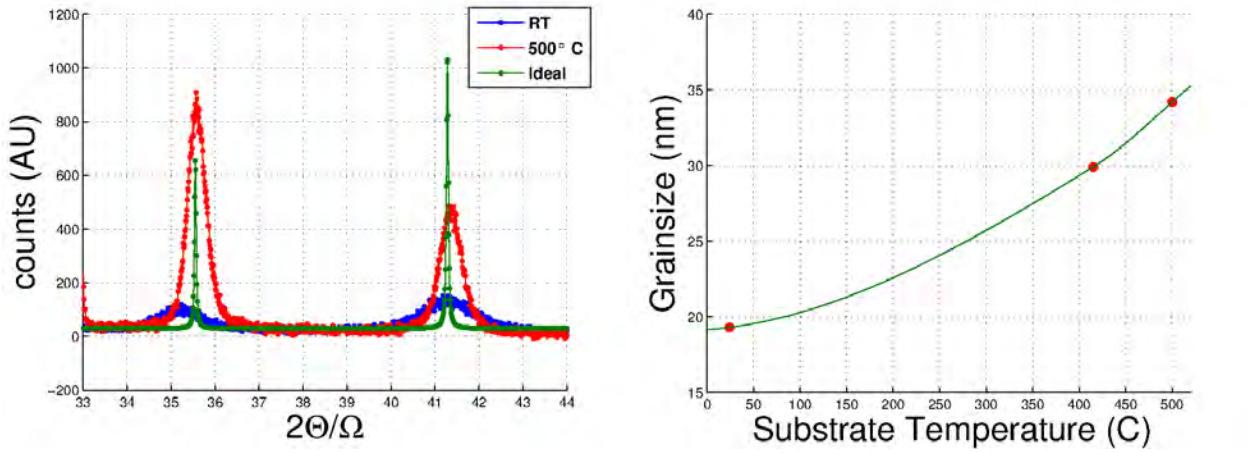

Figure 2.9: Left: X-ray diffraction pattern for NbTiN deposited at room temperature (RT) and 500 C. Also plotted is the powder diffraction pattern obtained by simulating the crystal structure using VESTA. Right: Temperature dependence of grain size, determined by AFM, for RBTIBD NbTiN films.

2.3.3 XRD Analysis

XRD analysis was performed on the two samples deposited at 3 SCCM flow rate at room temperature and 500 C, and a powder diffraction simulation was performed using VESTA [18]. The resulting XRD spectra are shown in Figure 2.9. Both the (111) peak near 35 degrees, and the (002) peak near 41 degrees for FCC NbTiN were observed, and agree with the powder diffraction simulation. A sharp increase in both the (111) and (002) peak height (indicating increased crystallinity) and a preferred (111) orientation are observed for the hot-deposited film. The effects of substrate temperature on grain size, determined through AFM, is shown in Figure 2.9- the increased grain size with increased substrate temperature is in agreement with the increased crystallinity observed in the XRD spectra. Using the (002) peak, a lattice constant of 0.436 nm is calculated, which corresponds to a nearest neighbor spacing of 0.308 nm in the closed packed (111) plane. This produces a near 3% lattice mismatch with our Wurtzite phase AlN. We note, shortly after this measurement, the X-ray diffractometer underwent maintenance and repair, and additional samples could not be analyzed during the time-frame of this study.

2.3.4 NbTiN/AlN/NbTiN Trilayer Deposition and I-V Characteristics

Two NbTiN/AlN/NbTiN trilayer samples were deposited at room temperature by RBTIBD; the base and counter-electrodes thicknesses were 200 and 100 nm respectively and the AlN barrier thicknesses were estimated to be 1.5 and 2.0 nm respectively. SIS junctions were fabricated using our Al-quadlevel test mask process and I-V data recorded through dip testing in liquid helium described in greater detail elsewhere [11]. The typical I-V characteristics of the two samples are shown in Figure 2.10. The sample with the thicker AlN barrier has a sum-gap voltage (taken at half the quasi-particle current rise) of 5.0 mV, a Jc of 6.7 $\frac{A}{cm^2}$, and $\frac{R_{sg}}{R_n}$ ratio of 18. The second sample with the thinner AlN barrier has a sum-gap voltage of 4.7 mV, a Jc of 1.0 $\frac{kA}{cm^2}$, and $\frac{R_{sg}}{R_n}$ ratio of 10. Notably, these results are the first ever reported for all NbTiN SIS junctions created with direct barrier deposition, and the highest sum-gap voltage reported for NbTiN based SIS junctions at the time of writing. While the current density is lower than the Nb/Al-AlN/Nb junctions previously reported by our research group, as we took a conservative approach for the first attempt at realizing RBTIBD all-NbTiN junctions, the Jc of 1 $\frac{kA}{cm^2}$ is not far from current SIS mixer designs, such as ALMA Band-6 design of 5 $\frac{kA}{cm^2}$ [19]. What is most remarkable and unique about the characteristics of the all-NbTiN trilayer is the high sum-gap voltage of 4.7-5.0 mV (gap frequency of 1.1-1.2 THz) indicating the potential future use in ALMA receiver designs, such as a optimal second generation ALMA Band 9 and Band 10 and may provide a technical path for future ALMA Band 11.

2.4 Summary and Future Work for Integration into ALMA

In the original proposal, we summarized the first research goal as, "A study of the suitability of an alternative materials deposition technology – Reactive Bias Target Ion Beam Deposition (RBTIBD) –that offers unique capabilities to tailor materials and interfaces, to realize all

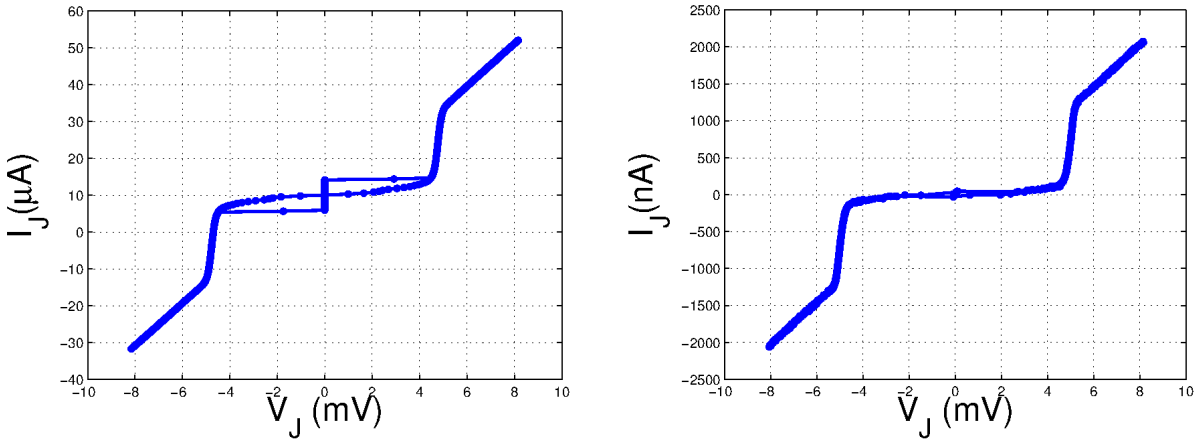

Figure 2.10: Typical characteristics of our RBTIBD all-NbTiN SIS junctions. Left: 1 $\frac{kA}{cm^2}$ 1.2 μm diameter SIS junction. Right: 6.7 $\frac{A}{cm^2}$ 3.2 μm diameter SIS junction.

NbTiN, higher energy gap (hence higher frequency) SIS devices needed for optimal second-generation Band 9 and Band 10 receivers and to provide a technical path forward for a future Band 11 receiver." We now report on the first ever all-NbTiN SIS junctions deposited by RBTIBD with low leakage currents and the highest reported sum-gap voltages for NbTiN based SIS junctions at the time of writing, a noteworthy and outstanding success with respect to our stated research goals.

A continuation of this one year exploratory study, would aim to further improve the quality of our all-NbTiN SIS junctions, and increase the current density to provide a technical path for integration into future ALMA SIS mixer designs. We observed that through heated deposition, we can improve overall film quality through decreased film stress, surface roughness, resistivity, and increased transition temperature and in-turn increased energy-gap. Additionally, by varying the inherent film stress of the NbTiN films through heated deposition, it may be possible to better tailor the lattice constants to better lattice-match and promote epitaxial growth of the AlN tunnel barrier. Future studies of the effects of deposition conditions on lattice constant through XRD and heated deposition of NbTiN/AlN/NbTiN trilayer will be an integral part to realizing higher current density all-NbTiN SIS junctions.

Whole Wafer Cryogenic Screening

3.1 Motivation

After completing fabrication of an SIS mixer wafer, one would next proceed to the post processing of individual mixer chips (for quartz architecture, this typically requires the very labor intensive thinning and dicing of the wafer into finished chips), mounting in a mixer block, and then cooling the receiver dewar in order to DC evaluate the SIS junctions. However, this is a painstaking and time-consuming evaluation route. Instead, the typical first line of electrical evaluation of a finished SIS wafer is performed by dipping finished chips into a liquid helium storage dewar. A small number of individual chips can be mounted on a carrier substrate and electrically connected (typically wire bonded) to a four wire test circuit that is then wired to a probe 'stick' and dipped into the liquid helium for SIS I-V testing. After dip testing has confirmed a reasonable yield of acceptable SIS junctions, one will proceed with the preparation, mounting and evaluation of actual mixer chips in the mixer block. Ideally, however, a wafer of mixer chips could also be DC evaluated in a simpler screening process and the selected chips, with now known electrical characteristics, used in the receivers. This is particularly important for ALMA with its large number of receivers and increasingly sophisticated mixer architecture of balanced and or sideband separating mixers that require multiple matched mixer chips. The above wire bonding screening approach can be used on individual chips, though for quartz architecture the chips must still be lapped-thinned and

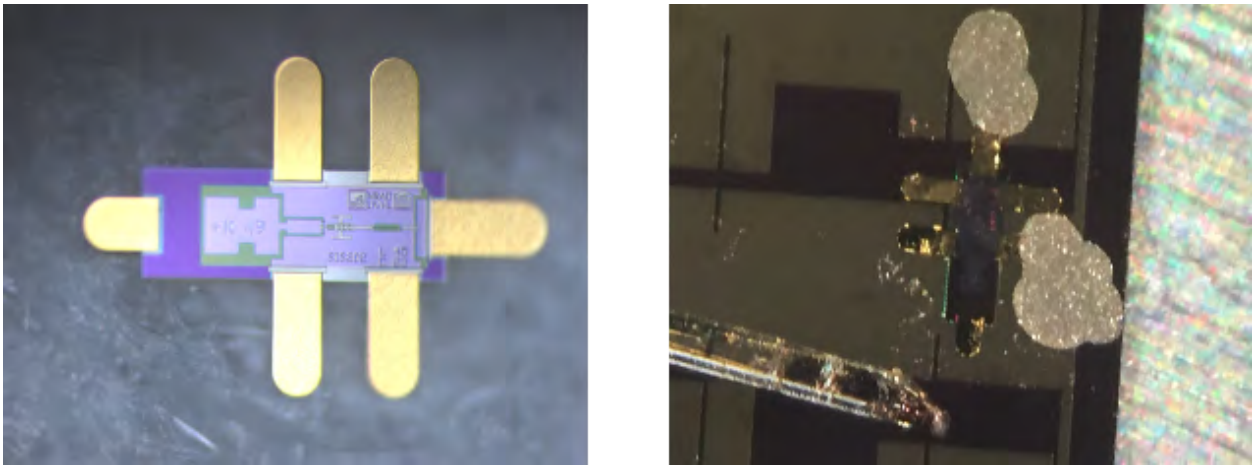

Figure 3.1: Left: Finished Band-8 UVML-NRAO 3 μm SOI Si mixer chip with 2 μm Au beam leads. Right: Band 8 mixer chip mounted with silver paint to a quartz test carrier. Applicator tool shown in lower left.

one must be careful not to damage the chip or gold contact pads. For our SOI architecture, individual ultra thin Si chips (Figure 3.1) are damaged by wire bonding. In collaboration with NRAO, a mounting process using silver paint or one component of a conductive epoxy has been developed to mount the SOI chips to an electrical carrier (Figure 3.1) where the conductive mounting medium is later dissolved with a solvent to release the intact mixer chip. However, such a chip-by-chip screening approach is still very time intensive, requires additional processing of the mixer chip to its final thinned form before evaluation, and is not practical for screening an entire wafer of thousands of chips.

The second thrust of the ALMA development study was toward the development of an all-wafer SIS device cryogenic screening method to address the challenges of the chip screening bottleneck. Realizing on-wafer cryogenic DC probing of SIS wafers would be an enormous benefit to all ALMA superconducting receiver programs. Such screening would allow quick verification of a wafer, rejection of inferior devices, the important matching of similar device characteristics in a balanced receiver design, and a feasible path toward populating receiver arrays with suitable mixer chips. For SOI wafers, it would additionally allow for frontside screening of the wafer before proceeding to the several weeks-long, labor and tool intensive backside wafer processing.

Our laboratory is equipped with a Lake Shore Cryotonics four arm CRTTP6-4K probe station capable of loading 51 mm and smaller sized wafers and chips. Experiments have been conducted using this tool to probe our SOI 3 μm thick mixer chips. The best electrical measurement results obtained with this tool are shown in Figure 3.2, where the I-V characteristics are plotted for different measured cold stage temperatures. This chip had been previously verified to posses a low leakage current and sharp turn on voltage from testing using the silver-paste and liquid helium dip approach. Clearly this I-V curve obtained by cryogenic probing indicates that the SIS chip temperature is higher than the 4.2 K substrate platter temperature. The probing of the device has warmed the temperature of the device above the platter temperature. From BCS theory evaluation of the reduced energy gap, we calculate the actual chip temperature to be 7.5-8 K. With a platter temperature of 7.9 K, the I-V curve reveals the Nb films to be in a non-superconducting, purely resistive state. Further experiments with the probe station reveal that the while the wafer platter obtains a low 4.2-4.3 K temperature, the Lake Shore DC probes are typically at a relatively warm ~15-20 K. Figure 3.2 is our best result; for some chips we see a resistive trace even at a 4.2 K platter temperature. These 'warm' probes, when landed to probe the chip, warm the chip $\geq$ 3 K above the platter temperature (as well as cool the probe 1-2 K). For our past iARPA JMRAM superconducting memory project, the leading manufacturers of cryogenic probe stations (Lake Shore, Cascade Microtech, MicroXact, MDC, ARS etc.) were contacted, however, there are no commercial systems that can realize a probed device temperature as low as the desired 5.5 K.

In this study, we investigated and optimized the thermal design/connections and heat management of our existing Lake Shore cryogenic probe station, and designed and fabricated improved DC cryogenic wafer probes. We first present the study of the thermal interfaces in our system using a differential thermal resistance measurement technique, from which it was found that many of these interfaces were non-optimal. Based on these results, we discuss the design, and evaluation of our improved DC cryogenic wafer probe. Using our custom made

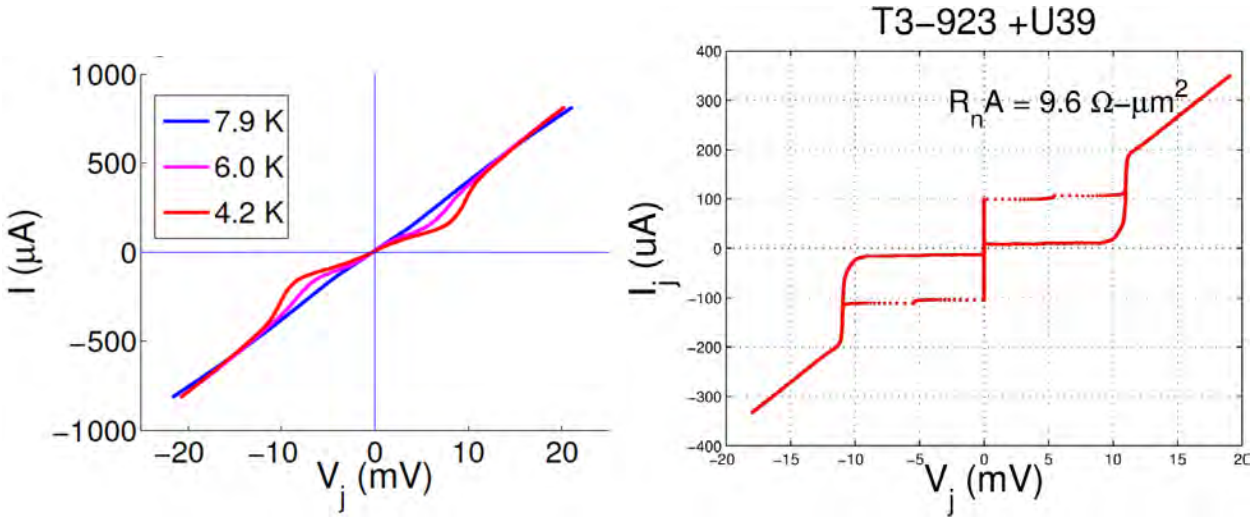

Figure 3.2: Left: I-V characteristics of a Band 8 mixer recorded in our cryogenic probe station plotted for different cold stage temperatures. Even with a cold stage temperature at 4.2 K, clearly the SIS chip temperature was significantly higher, yet below the 9.2 K T_c of the Nb films. Right: I-V characteristic of a Band 8 mixer mounted to our quartz carrier with silver paint and tested by submersion in liquid helium.

DC probe, we present the first ever on-wafer record Nb-based SIS I-V curves with a device temperature below 5.5 K at the UVML.

3.2 Evaluation of Thermal Interfaces

A top-level schematic of the probe station thermal connections, and a picture of the 4 stock ZN50 DC probe cards is shown in Figure 3.3. The room temperature probe arm assembly is allowed motion in the vacuum chamber via a bellows assembly. There are three separate shield stages nominally cooled to 30 K, 15 K and 4.2 K. The probe arm consists of a long hollow G-10 fiberglass insulating tube, a transition section that is covered in a copper jacket that is heat sunk to the 15 K stage, and a copper end socket fixture that is heat sunk to the 4.2 K stage. The DC probe card is integrated to a copper probe holder (bottom of Figure 3.3) with a rod on one end; the rod slips into the copper socket at the end of the probe arm and is secured with a setscrew.

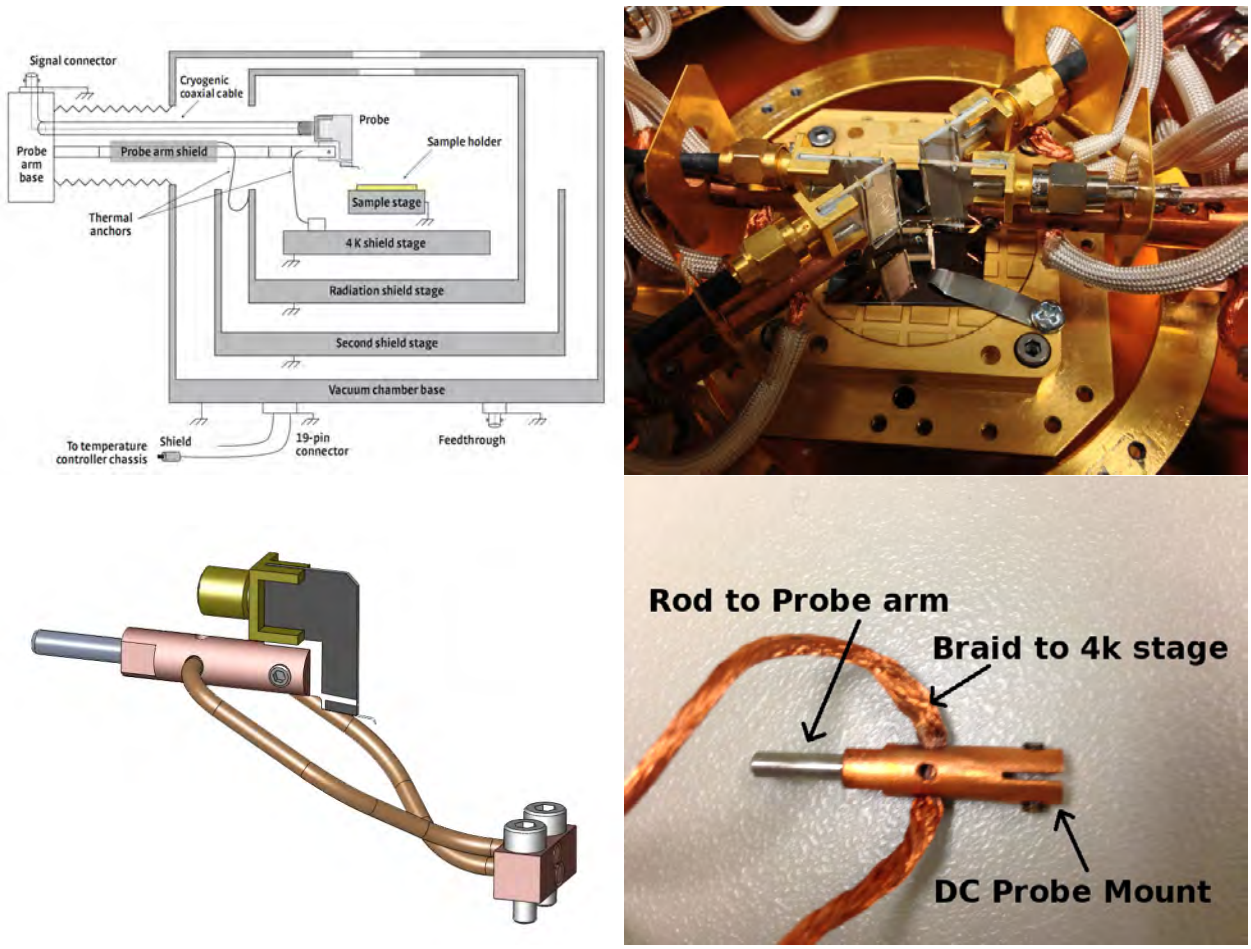

Figure 3.3: Top left: Top-level thermal schematic. Top right: Picture showing the four DC probe cards positioned above the sample stage. Bottom left: CAD view of assembled DC probe card. Bottom right: The DC probe card is inserted in the slot of the copper probe card holder and held in place with a pair of set screws.

3.2.1 Experimental setup

In order to investigate and improve the thermal management of our probe station and probes, a figure of merit and quantitative method to evaluate the thermal joints and heatsinking cables/straps is required. One such figure of merit the differential thermal resistance described in an NRAO EDTN [20]. We note our probe station is an open cycle design, meaning it consumes liquid helium during use. The cost and delivery time of liquid helium places a practical limit on the number of cool down cycles, and duration of each experiment– the use of an open cycle system was impractical for the number of measurements and experiments performed in this study. For this reason our closed cycle cryostat was used to evaluate individual aspects of our probe station through a series of experiments.

Figure 3.4 shows a sketch and a picture of our test setup. Our test setup consists of a gold plated copper metal block with an attached 200 Ω 5 W resistor to simulate a probe body with a heat load. The block is heatsunk to the 4 K stage of the cyrostat (based on a Sumitomo RDK-415D 4K Cryocooler) with copper braids, and is thermally isolated from cold stage with a G-10 fiberglass standoff. The copper braids are soldered into copper blocks at each end, and connections are made via bolted connections using a pair of M3x50 screws tighened to 70 cNm. A total of 4 Lake Shore DT-670 Si diode temperature sensors are mounted the 4 K stage (sensor 1), metal block (sensor 4), and on top of the copper blocks on each end of the braid (sensor 2 near 4 K stage, sensor 3 near metal block). With the cryostat cold, the differential thermal resistances were measured by applying a series of incremental heater power levels from 25 to 500 mW in 25 mW steps, and recording the temperatures at each power level after letting the temperatures stabilize for 5 minutes using code written in Python. The differential thermal resistance was calculated as

$$R_{P_N} = \frac{(T_2 - T_1)|_{P_N} - (T_2 - T_1)|_{P_{(N-1)}}}{P_N - P_{(N-1)}} \tag{3.1}$$

where T_1 and T_2 are the readings of two temperature sensors 1 and 2, and P_N and P_{N-1}

are consecutive heater power settings [20]. With the placement of the 4 DT-670 temperature sensors show in Figure 3.4 and noting Eq 3.1, the thermal resistance of the copper block to heated metal block interface using sensors 3 and 4, the braid assemble using sensors 2 and 3, the copper block to 4 K stage interface using sensors 1 and 2, and total thermal resistance from the metal body to 4 K stage using sensors 1 and 4, can be measured. This setup, with slight modifications when required, was used to investigate the following four areas:

1. **Heat sink cables bolted connections:** The effects of gold plating and the use of Apiezon N-grease on the bolted connections were investigated.

2. **Cable material:** We measured and compared the thermal resistance of the 'stock' copper braids provided by Lake Shore to Oxygen Free Copper (OFC) braids.

3. **Wafer mounting:** A new sample stage was designed, fabricated, and installed in our probe station, and the effects of the use of N-grease as a thermal interface material (TIM) between the sample stage and 51 mm wafer were investigated, as well as the possibility of gold metalization of the backside of the wafer.

4. **Design and comparison of custom DC probe to Lake Shore ZN50 DC probe:** A custom DC probe was designed and fabricated, and is directly compared to the Lake Shore ZN50 probe.

3.2.2 Heat Sink Cables and Bolted Connections

The standard DC probes shown in Figure 3.3 are generally heat sunk to the 4.2 K shield in the probe station using a pair of 15 cm long ~2 mm diameter copper braids. The copper braids are soldered to the probe card holder and a 6.3 x 6.3 x 14.5 mm copper block that is bolted to the 4 K stage by 2 M3x50 screwed tightened to 70 cNm. We note, the stock copper blocks that make the bolted connection are not gold plated. Two questions that arose with small bolted connections are (a) whether or not to use a TIM such as Apiezon N-grease

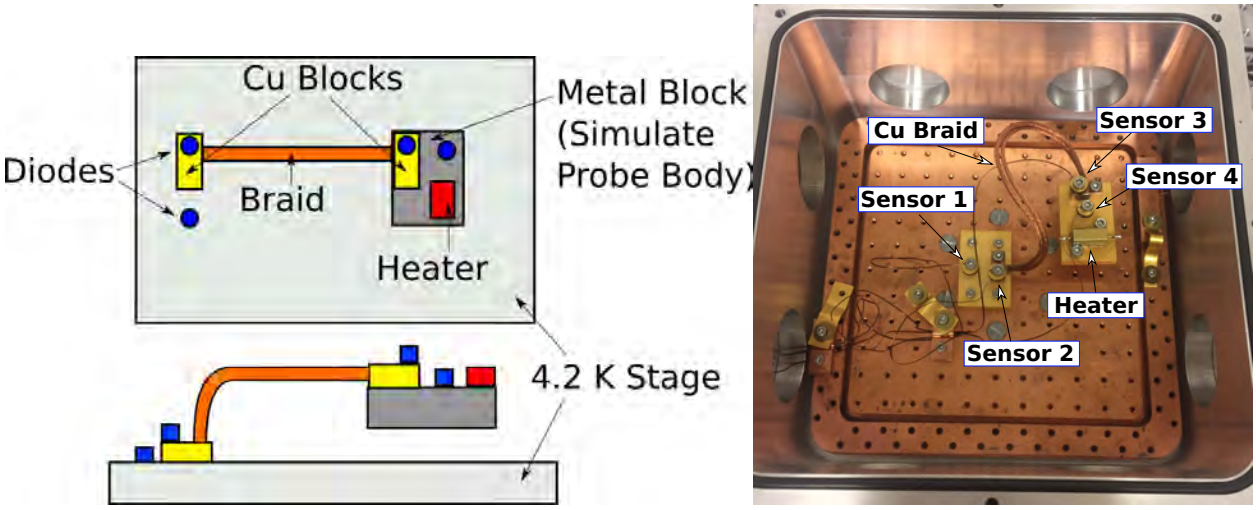

Figure 3.4: Left: Sketch of our differential thermal measurement setup. Right: Image of our measurement setup using our closed cycle cryostat. Note, because the 4 K stage is not gold plated, a 75 x 50 mm, 6.35 mm thick gold plated copper stage is permanently fixed to the center of the 4 K stage to make repeatable thermal connections, and is what we refer to as the '4 K cold stage' in our experiments.

at the mating surface, and (b) if gold plating offers appreciably lower thermal resistance compared to bare copper.

Two test structures consisting of two 15 cm long copper braids with similar copper blocks soldered to each end were fabricated to measure the thermal resistances of the copper braids as well as the bolted connections. One of the test structures had both of the copper blocks plated with 2.5 μm of Au. The total thermal resistances from the heated metal block to the 4 K stage plotted as a function of T_{hot}, the temperature of the heated metal block, for both gold plated and unplated bolted connections, with and without the use of N-grease are shown in Figure 3.5, as well as the individual thermal resistances for one of the test structures.

For both the gold plated and unplated bolted connections, the use of Apiezon N-grease showed little effect on the total thermal resistance of the strap, however a clear improvement is obtained through gold plating the interfaces for the bolted connection. The individual thermal resistances of each interface are plotted as a function of T_{hot} for one of cables in Figure 3.5– the total thermal resistance is clearly dominated by the thermal resistance of the cable. In order to reduce the thermal resistance of our heatsinking cables, alternative

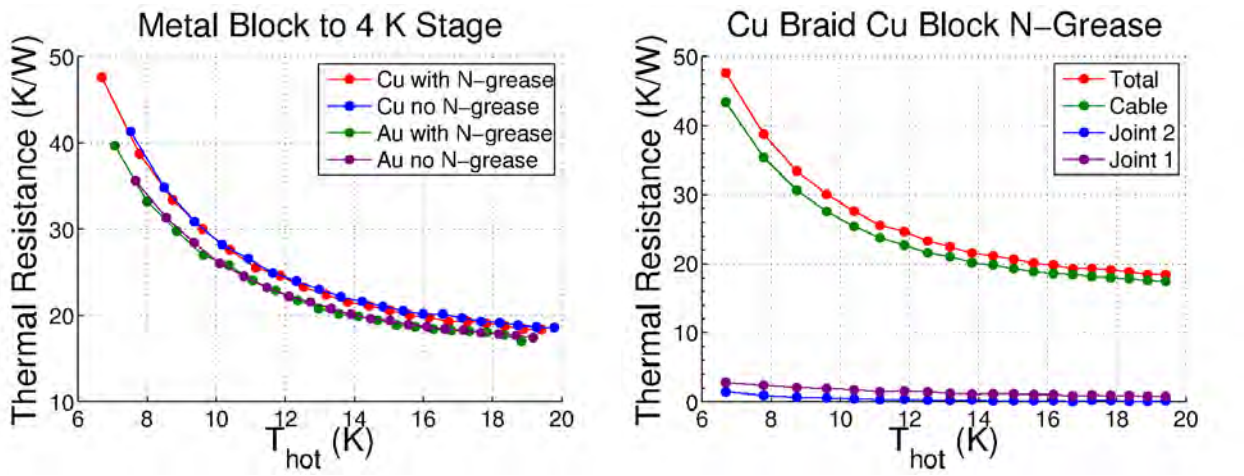

Figure 3.5: Left: Thermal resistance of entire stock strap, comparing gold plating and N-grease. Right: Individual thermal resistances of the unplated copper bolted connections with the use of Apiezon N-grease (stock setup used in our probe station), clearly showing the majority of the thermal resistance is due to the copper braids.

materials, such as OFC, were considered.

3.2.2.1 Choice of Heat Strap Material

Figure 3.5 indicates the majority of the thermal resistance from the simulated probe body to the 4 K stage is dominated by the copper braids, and not the bolted connections. Little information of the copper braid material provided by Lake Shore is given, but it not believed to be OFC. Similar ~2 mm diameter braids made from Copper Alloy-10100 99.99% min purity copper were obtained from Copper Braid Products, and an additional heat strap identical to the ones tested in the previous section was fabricated. Additionally 0.37 mm thick 6.35 mm wide gold plated annealed OFC solid straps were obtained from the NRAO Central Development Laboratory and tested. The thermal resistance of a single 15 cm long OFC copper braid and 72 mm long strap, are plotted in Figure 3.6 along with a single 15 cm long standard copper braid used in our probe station.

The annealed copper strap provided by NRAO demonstrated the lowest thermal resistance, however, due to it's stiffness and lengths provided, is not suitable for use with a movable DC probe, and will be limited to heat sinking of fixed non-movable parts. Further-

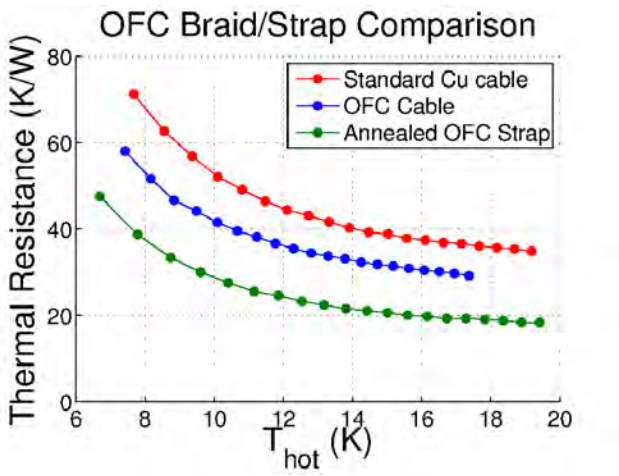

Figure 3.6: Thermal Resistance of single OFC braided cable and OFC strap compared to stock copper braid used in our probe station.

more, the improvement in thermal resistance obtained through annealing copper is reduced through introduction of defects when the strap is bent [21]. The OFC braid showed an appreciable improvement in thermal resistance, and since it is approximately the same dimensions as the stock braid used on our commercial DC probes, should allow the same freedom of movement and will be used in our new probe design.

3.2.3 Wafer Mounting and Sample Stage

A typical sample stage used in our probe station consists of a removable waffle patterned sample holder that is mounted to a fixed gold plated 4.2 K cold stage via a bolted connection. The sample is held in place via metal clips using the tapped mounting holes on the perimeter of the sample holder. A replacement stage, shown in Figure 3.7, was designed and machined from a solid piece of OFC. The removable sample holder was eliminated from the design, to remove an unnecessary thermal interface, and the waffle pattern was replaced with a mirror finish polished gold plated surface to increase wafer to stage contact area. The wafer is held in place with a gold plated clamp, using the 9 tapped holes on the perimeter to apply uniform pressure along the perimeter of our wafer. A wafer mounted to the entire assembled unit inside the probe station is shown in Figure 3.12 in the next section.

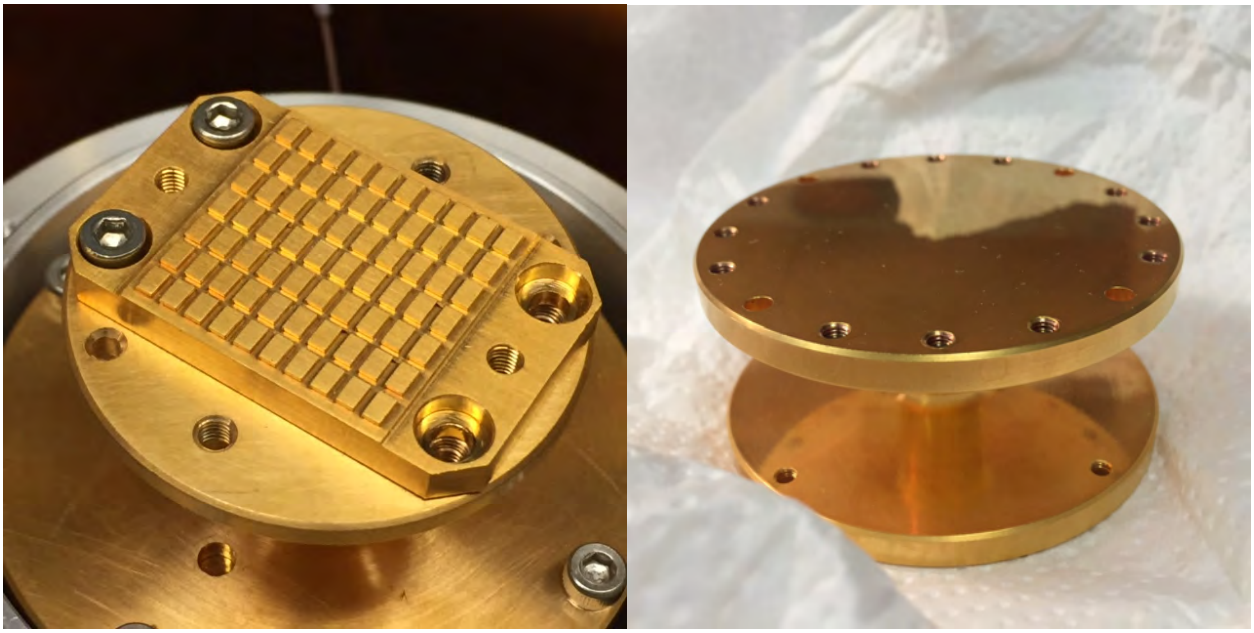

Figure 3.7: Left: Typical two-part sample stage with removable waffle-patterned sample holder. Right: New sample stage machined from a single piece of OFC designed as part of this study.

The use of N-grease as a TIM between the wafer and the sample stage was investigated, as well as the possibility of gold metalization on the backside of our wafers to provide a gold to gold interface between the wafer and cold stage. Two samples were prepared for this experiment, both consisting of 450 μm thick, 51 mm diameter (100) Si wafers with 250 nm of thermally grown oxide. Both samples had one side gold plated (to make repeatable connections to temperature sensors and the gold plated ring clamp), and the second sample had the backside gold plated, to provide a gold to gold interface to the sample stage. In our closed cycle cryostat, a mock stage was fabricated from an gold plated 6.35 mm thick OFC plate, to exactly mimic the surface and bolt patterns of our sample stage shown in Figure 3.7. A 200 Ω 5 W resistor was mounted to our ring clamp using Stycast® Epoxy 2850-FT, Catalyst 9, and a DT 670 temperature sensor was attached to the ring clamp and sample stage via a bolted connection. Similar to the differential thermal resistance experiments described earlier, incremental heater loads were applied and temperature recorded to measure the thermal resistance between the heated ring clamp and sample stage.

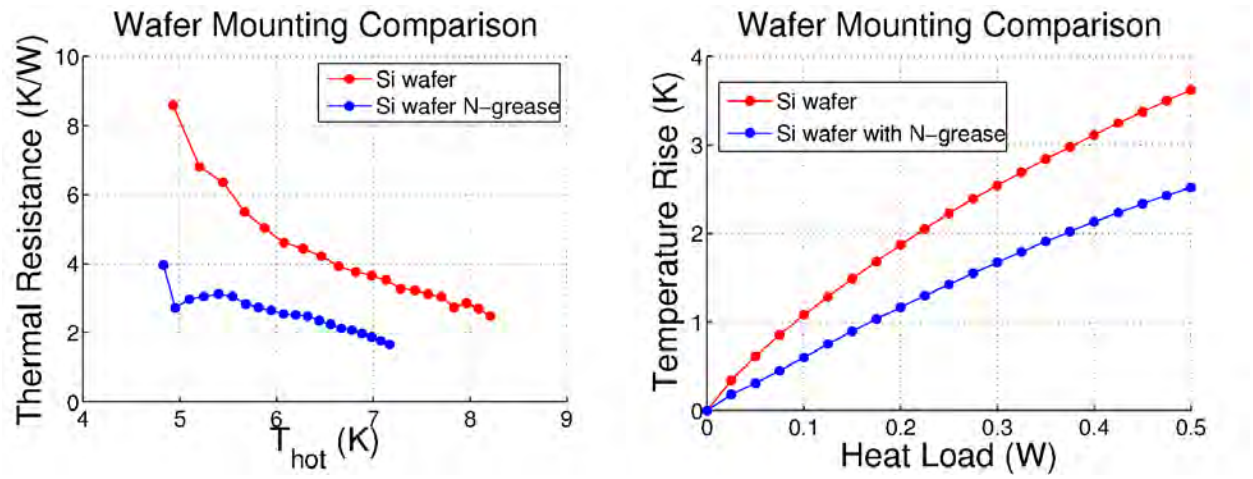

Figure 3.8: Differential thermal resistance as a function of T_{hot} and temperature rise (base temperature for both samples was 4.6 K) as a function of heat load for wafers mounted with and without Apiezon N-grease.

Figure 3.8 shows the thermal resistance as a function of T_{hot} for the non-gold-plated backside wafer with and without N-grease, as well as the temperature rise as a function of heat load. A near factor of 2 higher thermal resistance is observed for the wafer not using Apiezon N-grease as a TIM, and similarly, for a given heat load a larger temperature rise is observed. The gold backside plated sample formed a bond with the gold plated stage after applying pressure with the clamp, and the wafer broke while being removed. Additional tests using backside metalization of the wafer were not performed as the risk of breaking an actual mixer wafer during screening is too great. We concluded that the use of Apiezon N-grease is beneficial for our 51 mm Si wafers in our particular setup, and will be used for our wafer probing experiments.

3.2.4 Design and Fabrication of Custom DC Probe

A differential thermal resistance measurement was performed on the stock ZN50 DC probe shown in Figure 3.3. A 200 Ω resistor was attached to the SMA port of the probe card with Stycast epoxy, a temperature sensor was mounted to the probe card and copper probe card holder. A bolted connection was made to the 4 K cold stage, and a diode was mounted on

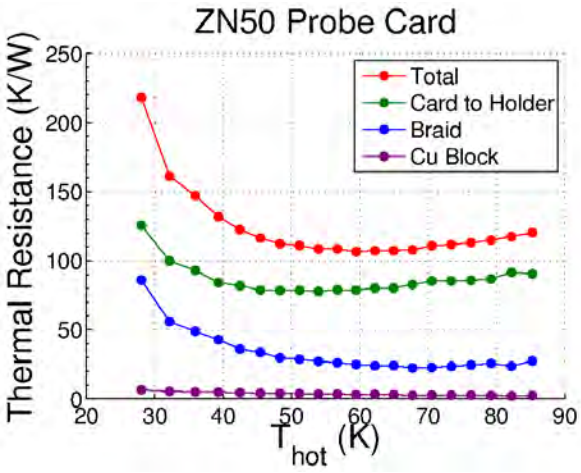

Figure 3.9: Differential thermal resistance as a function of T_{hot} of the various thermal interfaces of the stock ZN50 probe card.

both the copper block and cold stage. The thermal resistance measurements are shown in Figure 3.9.

The thermal resistance is dominated by the interfaces between the probe card and probe card holder. Noting Figure 3.3, the probe card rests in a slot milled into the copper probe card holder, and is held in place by two set screws. The two set screws provide the only physical path for heat conduction. Noting this, we set our design on a solid body metal probe, with the probe tips physically integrated into the metal block.

3.2.4.1 DC Probe design

Based on our previous results, we designed a prototype DC probe that utilizes a solid OFC body with integrated DC probes, OFC braids, and gold plated bolted connections to the cold stage. Each probe contains two independent probe tips to reduce the number of required probes, probe arms, and manipulators needed for a 4-point measurement from 4 to 2– reducing the thermal loading of the probe station and requiring manipulation of fewer probes. The CAD drawing of our probe design is shown in Figure 3.10. The probe body is machined from a single piece of OFC, two holes are milled through the body to accept OFC braids to be soldered directly to the body. A hole is machined in the rear of the probe to

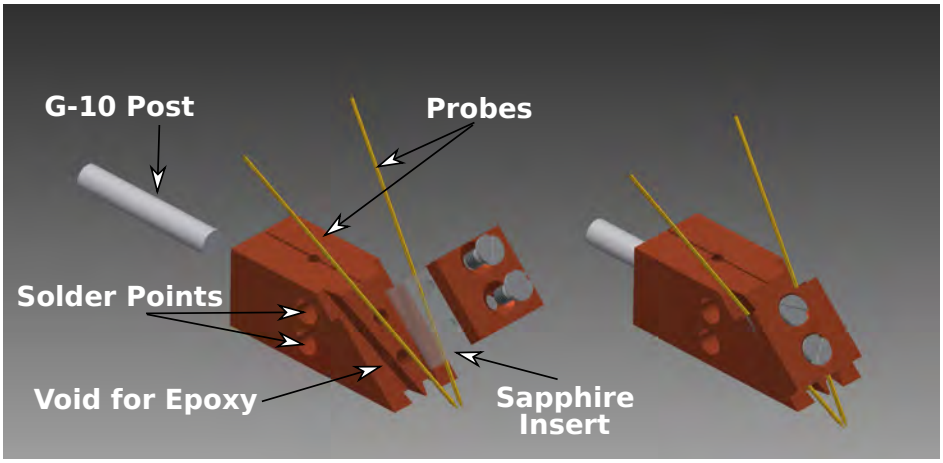

Figure 3.10: CAD view of the custom DC probe designed as part of this work. The 2 voids on the front face are filled with Stycast epoxy and the 2 gold plated tungsten probes sit in a machined slot in the epoxy and are held in place by a copper plate with a single crystal sapphire insert to prevent shorting. Copper braids are soldered directly to the probe body to provide cooling, and the probe is attached to the manipulator via a G-10 post to provide a thermal break.

accept a G-10 fiberglass rod to provide a thermal break when it mates to our manipulator's probe arm (Figure 3.3). Two gold plated tungsten probes must make physical connection to the probe body for proper heatsinking, yet be electrically insulated. Two voids are machined into the probe body, and they are filled with Stycast epoxy, which is both electrically insulating and a good thermally conductor at cryogenic temperatures, and two channels that match the 0.5 mm diameters of the probes are formed in the cured epoxy. The probes rest in the two channels and the Stycast epoxy prevents shorting of the probes to the copper body while providing a physical connection for heatsinking. The probes must also be held into place by a rigid piece that is also electrically insulating and a good thermal conductor at cryogenic temperatures. A single crystal sapphire insert was machined, and sits between the probe body/probes and a OFC clamp that is held in place by two machine screws. Electrical connections are made to the probe tips by a twisted pair of phosphor-bronze wire that are heatsunk to the probe body with GE 7031 varnish.

3.2.4.2 Thermal Measurements of Custom DC Probe

Two prototype DC probes shown in Figure 3.10 were machined and assembled at the UVML. Thermal resistance measurements were made for comparison to the stock DC probe card– a similar 200 Ω resistor and DT-670 temperature sensor were mounted to the probe bodies. We note that only 2 copper braids were soldered to the probe body for a fair direct comparison to the stock DC probe. The thermal resistances plotted as a function of T_{hot} measured from the two custom probes are shown in Figure 3.11. The results are consistent across both of our custom DC probes, measured during two successive experiments. We note that there is an additional plot for the stock ZN50 probe card as it was modified to improve the thermal contact between the probe card and probe card holder. One of the two set screws was removed and the remaining set screw was used to press the probe card against one side of the slot where Apiezon N-grease was applied. The modifications modestly reduced the overall thermal resistance of the stock probe, however, the custom machined probes have a near order of magnitude lower thermal resistance. The thermal resistance plots do not line up as a function of T_{hot}, this is because the same applied heat loads were used for all measurements, and the stock probes produced a higher T_{hot}, even at the lowest applied heat load. A visually better comparison is monitoring the temperature rise as a function of applied heat load, shown on the right side of Figure 3.11. A applied heat load that produced a ~40 K temperature rise in the best case scenario for the stock DC probe, produced a <10 K temperature rise in the custom DC probe, a notable improvement.

3.2.5 On Wafer SIS I-V Measurement Results

A wafer containing Nb/Al-oxide based SIS junctions was fabricated using the aforementioned test mask process. A small section of the wafer was removed with a dicing saw to allow dip testing of a few junctions to first verify the I-V characteristics of the SIS junctions before testing in the probe station. The wafer was then mounted into our Lake Shore probe station, along with the 2 UVA custom DC probes shown in Figure 3.12. DT-670 temperature sensors

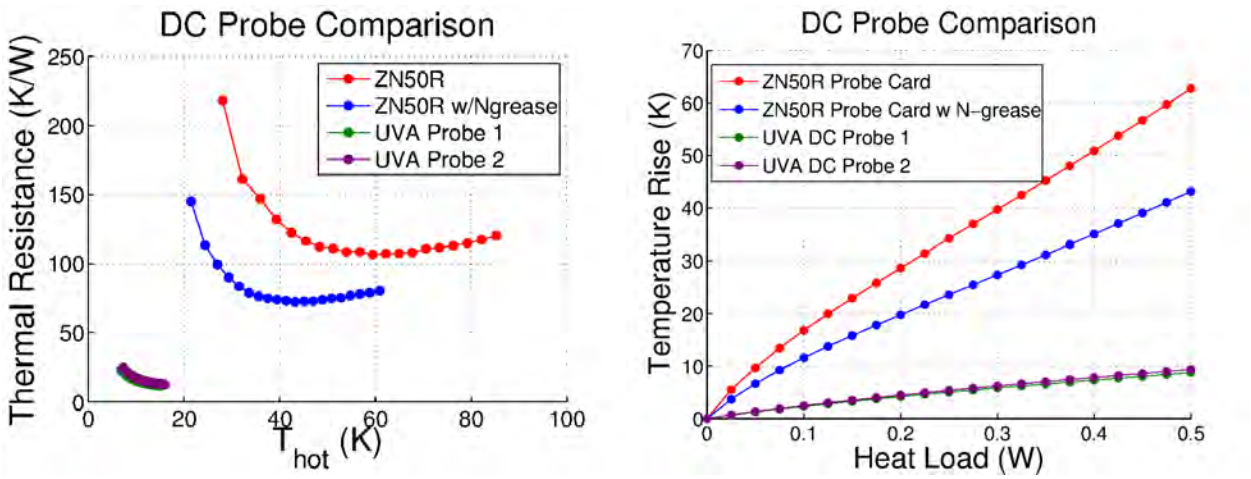

Figure 3.11: Left: Thermal Resistance of custom probes designed and machined at the UVML compared to the stock ZN50 DC probes. Right: Temperature rise plotted as a function of applied heater power.

were mounted to each probe body, the top of the ring clamp that secures the 51 mm wafer, and the 4 K radiation shield to which the DC probes are heatsunk. Temperature of all 4 temperature sensors were recorded during the cool down and are shown in Figure 3.13. After 30 minutes all temperatures begin to stabilize, and after 2 hours both DC probes were cooled below 10 K.

After both probes were cooled below 10 K, the DC probes were landed onto the gold contact pads on the wafer, and the I-V characteristics of the SIS junctions were recorded. Figure 3.14 shows the landed probe tips, as well as the I-V characteristic recorded on-wafer compared to those recorded by dip testing in liquid helium. The on-wafer recorded I-V shows a current rise that begins around ~2.65 mV; at 95% of the expected 0 K energy gap, BCS theory predicts an on-wafer device temperature of ~5 K.

3.3 Summary and Future Work for Integration into ALMA

In the original proposal, the second research goal was to create a whole wafer screening method for SIS mixers, by investigating and optimizing the thermal management of our Lake Shore cryogenic probe station, and ultimately designing and fabricating a custom cryo-

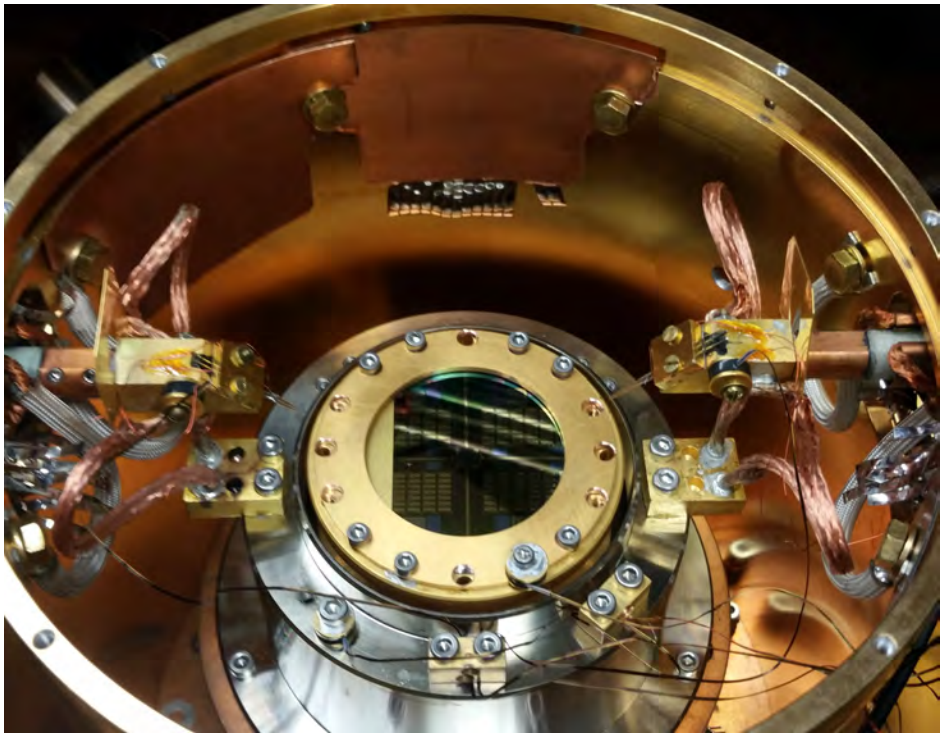

Figure 3.12: View of our modified Lake Shore probestation showing custom stage, wafer mounting ring clamp, and pair of custom DC probes.

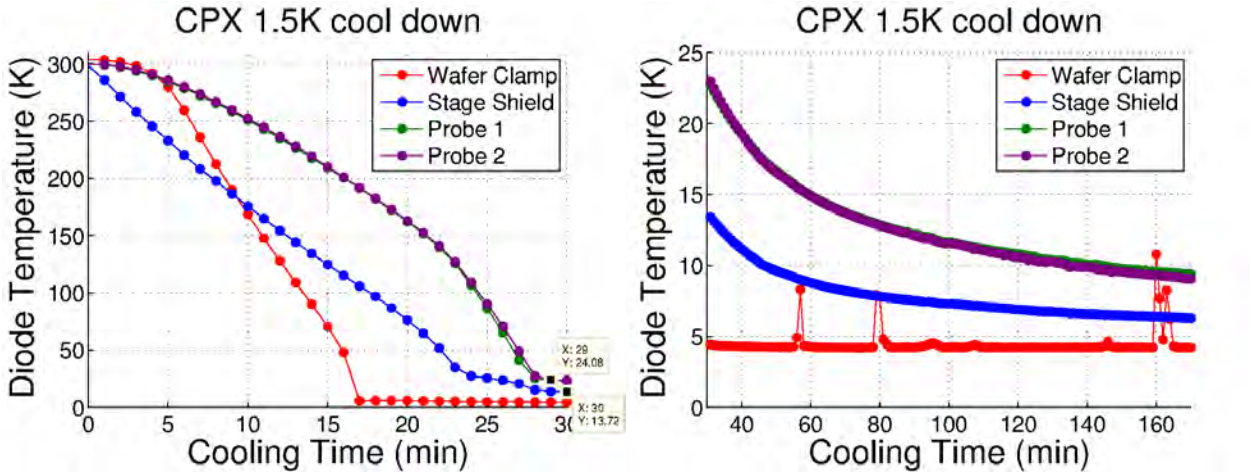

Figure 3.13: Temperatures recorded during the cool down of our probe station before testing. The spikes observed on the right are due to optimizing the liquid helium flow rate to reduce consumption.

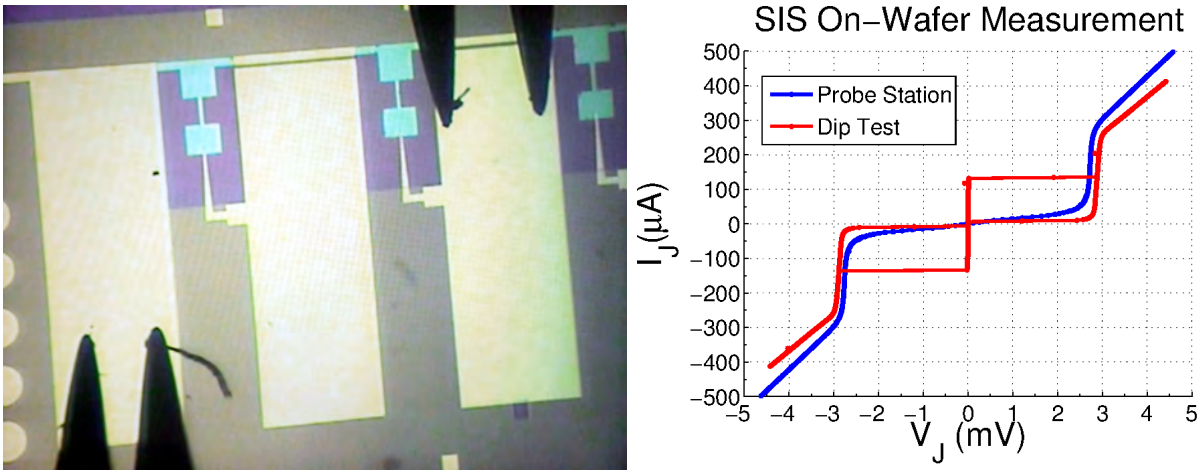

Figure 3.14: Left: Landed DC probe tips. Right: On-wafer recorded I-V characteristics plotted along side those recorded by dipping in liquid helium. The nominal diameter of both junctions are the same.

genic DC probe. Differential thermal resistance measurements of various thermal joints in our probe station showed some to be sub-optimal. Based on these results our probe station underwent modifications, and a custom DC probes were realized at the UVML with significant improvement over the stock DC probes, both in thermal management and reduced number of probes required to perform a four point measurement. Culminating from this research, for the first time at the UVML, we demonstrated the ability to non-destructively on-wafer measure the I-V characteristics of SIS junctions with device temperatures of ~5 K. This was achieved through modifications to our probe station and design of a new DC probe. In terms of our stated research goal, this was an outstanding overall success.

The demonstrated ability to measure SIS I-V characteristics on-wafer, if applied to the cryogenic DC screening of SIS wafers, will in turn enormously benefit all ALMA superconducting receiver programs, including the ongoing ALMA Study for a 2nd generation Band 6 receiver, and multi-beam receivers through ability to pick out the best desired mixers from a wafer. While we have demonstrated the ability to on-wafer characterize SIS junctions, we note that the positioning of the probe arms, and recording of the I-V data is a manual process, and applying such a process to a wafer containing 1000's of devices, while significantly faster than the current process of dip testing individual mixer chips, is still a very

time consuming process. Future work, to automate both the positioning of the probes, as well as the I-V data recording would be an enormous benefit to realizing full-wafer screening of superconducting devices.

The new DC probes, designed as part of this work, performed exceptionally well compared to the commercially available DC probes. The design utilized commonly used Micromanipulator 7B series probe tips; while these probe tips are suitable for testing SIS devices with large contacts pads (such as the test device wafer used in this study) the fairly large ~ 500 μm tip diameter may provide a challenge for testing actual mixer wafers with Au beam leads of similar scale. We also note, to provide a fair comparison and guarantee the same degree of motion of the original stock probes, that our custom DC probe only utilized 2 copper braids of similar diameter to the stock DC probe for heatsinking to the 4 K cold stage. It may be possible to obtain lower thermal resistance and cooler probe temperatures through use of either additional or thicker diameter copper braids. A second generation DC probe design, utilizing smaller diameter probe tips and improved heatsinking through additional and/or thicker copper braids could increase the ease of probing smaller mixer circuits and further decrease on-wafer device temperatures.

We also note additional care must be taken when handling SIS mixer wafers as the micron and sub-micro sized SIS junctions and circuitry are easily damaged during testing from high currents/voltages from biasing circuits and electrostatic discharge (ESD). Our commonly used SIS dip testing setup contains robust ESD and biasing protection through grounding, shielding, neutralizing ionizers, and filtering. During testing in our probe station, a few SIS devices were damaged, and future work to design an interface between the biasing circuit and probe station, to provide grounding and filtering, will minimize device damage in the future.

It was noted that our Lake Shore probe station is of an open-cycle design and consumes liquid helium during operation. Use of the probe station has to be scheduled around the delivery of liquid helium (typically delivered one day a week with a one to two week lead

time), and both the length and number of cool down cycles is limited by the amount of helium, typically a single cool down is achievable with a single 30 l liquid helium dewar. This may pose a problem for the time required to screen a full wafer, and it also limits the practical number of iterations when performing experiments, such as optimizing thermal connections and heat management of the system. The use of a closed-cycle cryostat was indispensable in this study for optimizing thermal management and thermal characterization of our DC probes. Modifying our Lake Shore probe station to a closed-cycle design would alleviate these conserves, and is one area for potential future improvement.

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