Towards a Second Generation SIS Receiver for ALMA Band 10

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Summary: This report describes work done towards a new generation of receivers for ALMA Band 10. While it is focused on Band 10, much of it could be applied to the other high-frequency ALMA bands, particularly Band 9 which, unlike the lower-frequency bands, do not currently have sideband-separating receivers. Section 1 describes the design of a basic mixer for Band 10 with improved noise temperature and bandwidth. While the required SIS junction technology is being refined we have used a half-frequency design (close to ALMA Band 8) to explore the design of a mixer using series-connected SIS junctions in a special low-inductance configuration. Section 2 explores a new approach to the elimination of trapped magnetic flux from SIS mixers with multiple junctions. The advantages of sideband separation are greatest in the higher frequency bands where the atmospheric contribution to the system noise is greatest. LO sideband noise can be a significant component of the system noise at some LO and intermediate frequencies, and this can be reduced substantially by using a balanced mixer configuration. There are several configurations possible for balanced sideband-separating mixers, and section 3 describes these and refers to the full discussion in a companion report. Section 4 discusses the importance of the mixer-to-IF amplifier interface, and also refers to the companion report.

1. SIS mixers for Band 10

Fig. 1 shows the single-sideband noise temperatures of the current ALMA receivers as a function of frequency [1]. As Bands 9 and 10 use double-sideband receivers, the equivalent SSB noise temperature, $2*T_{DSB}$, is shown for those bands. From this figure, it is clear that the Band-10 receivers differ from the others in two ways:

(i) They have relatively high noise temperature. This is due to the use of Nb/Al-AlOx/Nb SIS junctions above the energy gap frequency of Nb [2].

(ii) They have greater variation of noise temperature across the band than do the lower-frequency receivers. This is a reflection of the difficulty of making high-quality SIS junctions with low enough capacitance to allow a broadband matching circuit to be incorporated in the mixer.

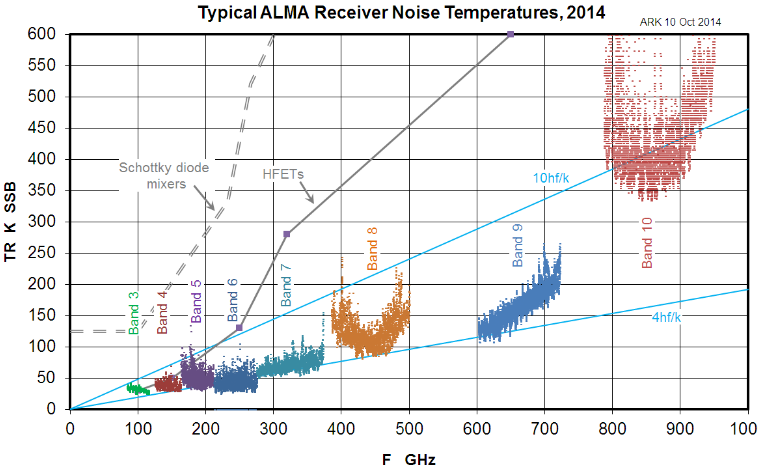

Fig. 1. Single-sideband receiver noise temperature vs frequency for typical ALMA SIS receivers. Bands 3-8 have sideband-separating mixers and Bands 9 and 10 have double-sideband mixers. The noise temperatures shown for the DSB receivers are twice the DSB temperatures. From [1].

In this study, we consider the design of mixers with NbTiN counter-electrodes whose higher superconducting energy gap increases the frequency limit above which the mixer performance degrades rapidly. We also consider SIS junctions with AlN tunnel barriers (as opposed to the AlOx barriers used in most current SIS mixers). Good quality Nb/Al-AlN/Nb SIS junctions have been made with critical current densities as high as 30,000 A/cm^2 as shown in Fig. 2. This allows the area to be reduced by a factor of 3 to 4, and the capacitance correspondingly reduced, while maintaining a desired junction conductance.

In 2007, Nb/Al-AlN/Nb SIS junctions were fabricated at UVML with critical current density as high as 30,000 A/cm^2 and high quality I(V) characteristics. Fig. 2 shows the I(V) curve for two such junctions in series. Apart from a slightly higher leakage current, the quality is as good as that of Nb/Al-AlOx/Nb SIS junctions with a fraction of the critical current density.

Also since 2007, UVML has fabricated small area Nb/Al-AlOx/NbTiN SIS junctions with a gap voltage of ~3.3 mV (cf. 2.8 mV for typical Nb/barrier/Nb SIS junctions) and high quality I(V) characteristics. Typical results are shown in Fig. 3.

For the next-generation Band-10 receivers the goal is to produce high-quality, highly reproducible, small area SIS junctions with AlN barriers and NbTiN counter electrodes – i.e., Nb/Al-AlN/NbTiN SIS junctions – and to design broadband RF matching circuits which will give flat operation over at least the 1.21:1 ALMA Band 10 (787-950 GHz). The development of these SIS junctions is under way at UVML. First it was necessary to improve the repeatability of the AlN barrier formation and further reduce the leakage current, and much of UVML's time on this project has focused on that [3]. In the mean time, we have concentrated on the development of an improved mixer chip and tuning circuit design for Band 10 using half-frequency-scale SIS mixers (approximately ALMA Band 8) with Nb/Al-AlN/Nb junctions.

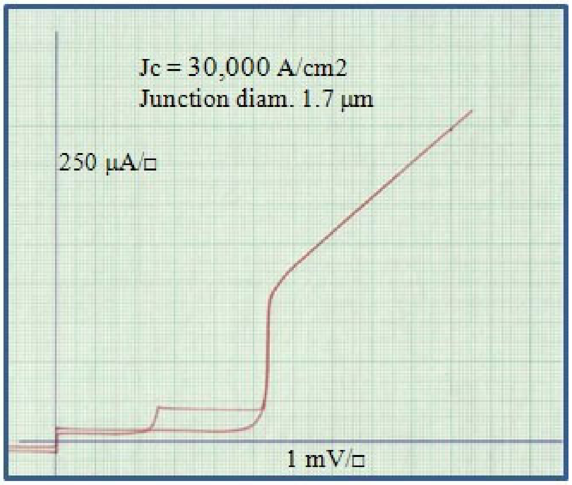

Fig. 2. I(V) characteristic of a series pair of SIS junctions with AlN tunnel barriers. The Nb/Al-AlN/Nb SIS junction has J_c = 30,000 A/cm^2 and was fabricated at UVML. [Lichtenberger, 2007]

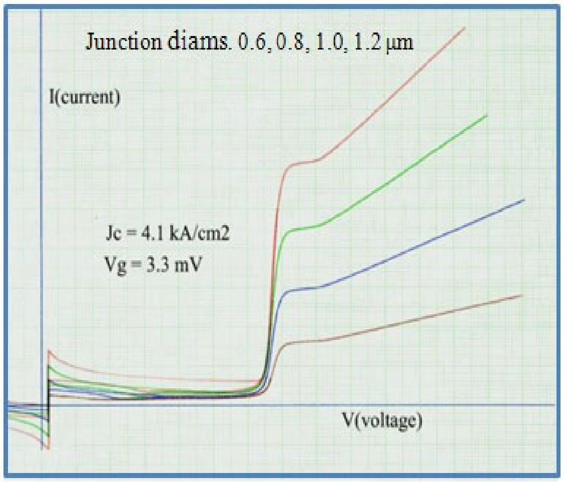

Fig. 3. I(V) characteristics of SIS junctions with one NbTiN electrode. The NbTiN/Al-AlOx/NbTiN SIS junctions have diameters 0.6, 0.8, and 1.2 µm, and were fabricated at UVML. [Lichtenberger, 2007]

A new type of substrate for sub-mm circuits:
The current ALMA SIS receivers use standard millimeter-wave technology with the SIS junctions and associated tuning circuits fabricated on a thick quartz substrate suspended across a waveguide. The thickness and width of the substrate are limited by the onset of higher mode propagation in the substrate channel. Simply scaling the Band 3 or Band 6 designs to Band 10 THz requires a substrate 20 µm thick x 60 µm wide. Even in the lower-frequency bands, mounting the quartz mixer substrates in waveguide blocks and making the DC, IF, and ground connections is difficult and has been a source of unreliability and variation in the performance of the mixers. A new process, developed at UVML, allows a mixer circuit to be fabricated on Si membrane only 3 µm thick, and suspended by gold beam-leads which also make the IF, DC, and ground connections. Fig. 4 shows a membrane and beamlead mixer chip for our half-frequency-scale developmental mixer.

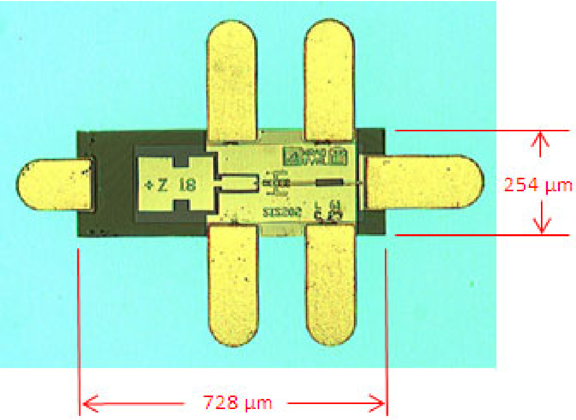

Fig. 4 Example of a Si membrane & beamlead SIS mixer for 385-500 GHz. The Si membrane (dark) is 3 µm thick and the gold beam leads are 2 µm thick. RF, IF, and DC ground connections are through the beamleads. The right-hand beamlead is the DC/IF connection and the short left beamlead is solely for mechanical support. The waveguide probe has the ID label "+Z 18"

Silicon membranes with gold beamleads are also used in our sub-mm LO couplers. Standard waveguide branch-line LO couplers require several deep but very narrow waveguide channels to be machined between two full-height waveguides. For Band 10, full-height waveguide is 140 x 280 µm and machining branch-line couplers is impractical. Coupling between the LO and signal waveguides in a mixer block can be accomplished using a Si-membrane coupler as shown in Fig. 5. The coupling can be adjusted between 20, 16, and 10 dB by using 1, 2, or 3 coupler sections.

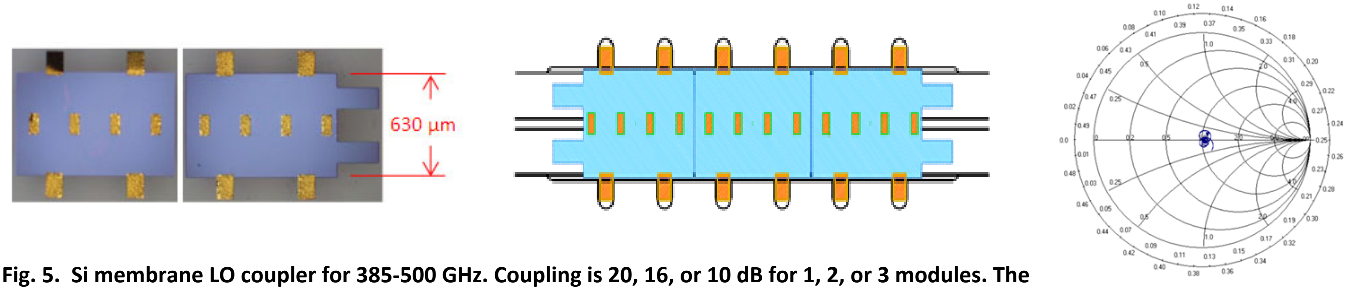

Fig. 5. Si membrane LO coupler for 385-500 GHz. Coupling is 20, 16, or 10 dB for 1, 2, or 3 modules. The Smith chart shows the reflection coefficient of the coupler across the full band.

These circuits are fabricated on a 3 µm Si membrane on a thick Si carrier wafer. Between the carrier wafer and the membrane is a thin etch-stop layer which allows the carrier wafer to be etched away without damaging the finished circuits on the membrane. When the membrane circuits are liberated in this way, they fall onto a filter paper, and they are delivered to us on the filter paper. This approach circumvents the laborious lapping and dicing procedure used with the first generation ALMA SIS receivers, and results in chips with much more precisely defined dimensions – important considerations for ALMA with its large number of receivers.

Membrane & beamlead mixer chip handling, DC testing, and storage

Handling, testing, and storing these tiny ESD-sensitive membrane circuits required new procedures. They are too delicate to store in a GelPak, and picking them up with tweezers is very risky even for the most experienced technician. Prior to using the membrane chips in a mixer, their I(V) characteristics are measured using a test mount which can be dipped directly into a liquid helium storage dewar. It is necessary to mount chips temporarily in the test mount and then return them to a labeled storage location. Several months were spent developing procedures, which now allow us to handle and store these chips safely.

(a) Chip storage and handling. The beamlead and membrane chips are conveniently stored in isopropyl alcohol. They can be shipped in IPA in small jars. After initial DC testing, they can be individually stored in antistatic plastic trays with numbered wells, like the one shown in Fig. 6 [4]. When they are in IPA, the chips can safely be picked up and deposited using a medicine dropper. For mounting in a mixer block or test fixture, it was found that the chips could be picked up relatively easily on the flat ground edge of a scalpel blade, as shown in Fig. 7. Wetting the blade first with isopropyl alcohol can be helpful, but when the chip is to be mounted in a mixer with conductive epoxy already applied, IPA should be avoided as it mixes with the uncured epoxy.

(b) Temporary mounting (with electrical connections). For DC testing, the membrane and beamlead mixer chips at 4 K, they can be mounted using only Part B of H20E[1] conducting epoxy. Part B contains enough silver platelets to make an electrical connection, although a small resistance, usually < 1 Ω, may be visible in the critical current region of the I(V) curve. Part B has sufficient surface tension to hold a chip securely even when dipped into LHe. Recently, we have learned of a silver-loaded silicone grease which may be better in this application than H20E Part B and we will soon be conducting tests using it.

Fig. 6. Antistatic cavity tray, ECP 4006-50BK tray and 4006-50FC-AS lid.

(c) Removing residual conducting compound. Before the mixer chip can be mounted in a mixer, any residual conducting compound must be removed. We initially thought this would be possible using acetone or IPA with ultrasonic agitation, but it was found that the ultrasonic agitation removed the gold beamleads, even when the ultrasonic power was reduced to the minimum required to remove the H20E Part B. Eventually it was found that a fine artist's brush (Round #0 [5]) could be used to scrub the chip in a dish of IPA, but it takes a lot of practice to avoid damaging the beamleads.

(d) Final mounting of the chip in a mixer block. Epotek H20E conducting epoxy is used to connect the beamleads to the appropriate contact pads in the mixer block. For the ground contacts (the four side leads) small channels are machined in the block, with a recess at the end of each to accommodate any epoxy which is squeezed out. Small drops of epoxy are applied and the chip put in place as described above. A microscope slide is placed on top of the block while the epoxy is cured to make sure the chip and beam leads do not protrude above the block surface.

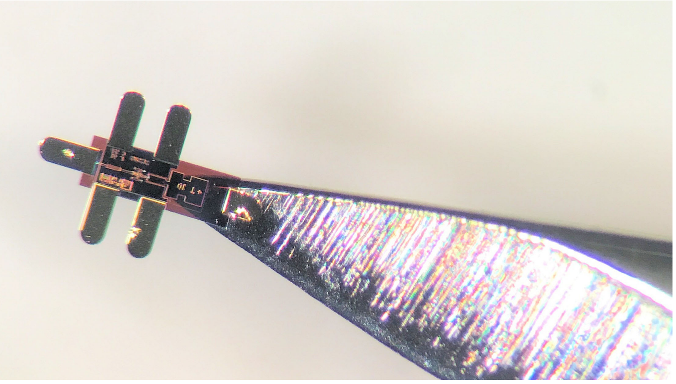

Fig. 7. A 385-500 GHz membrane and beamlead mixer chip can be picked up and moved on the edge of a scalpel blade.

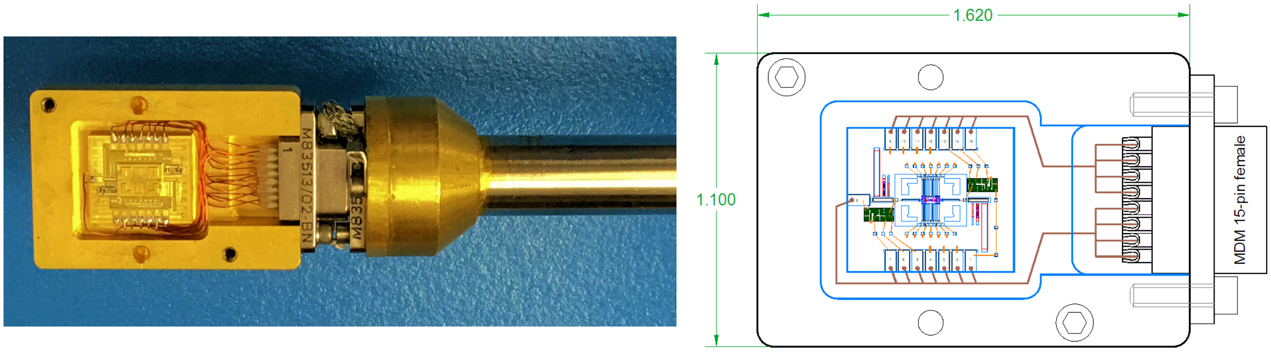

Fig. 8. The 4-K chip test mount attaches to a stainless steel dipstick for rapid I(V) measurements of mixer chips. Dimensions in inches.

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[1] Epoxy Technology Inc., www.epotek.com.

(e) DC testing. For rapid measurements of the DC I(V) characteristics of these small membrane and beamlead chips at 4 K, a dipstick was designed for insertion into a LHe storage dewar – Fig. 8. This avoids the long cool-down and warm-up times for a refrigerator based test system. The chip mount contains two SIS bias chips – RC networks with a current-sensing resistor and ESD protection, which allow accurate 6-wire measurement of the I(V) characteristics. It can measure chips of several sizes, two at a time.

Mixer circuit design

It is planned to use Nb/AlN/NbTiN SIS junctions for the new Band 10 mixers. As explained above, while the fabrication process for these junctions is being refined, our initial development has been done using half-frequency-scale SIS mixers (approximately ALMA Band 8) with Nb/Al-AlN/Nb junctions. The mixer design is in many ways similar to those used for ALMA Bands 3 and 6, as described in [6], in which four junctions were connected in series. The use of a series array of junctions in an SIS mixer has two advantages compared with a single junction. For the same overall impedance level, the individual junctions of the array are larger, which makes them easier to fabricate consistently and with high-quality I(V) characteristics. Also, the dynamic range (or saturation power) of an SIS mixer, which depends on N^2f^2, is greater. In the present work we have used four junctions in series for the half-frequency design and two junctions in series for the Band-10 designs.

The RF bandwidth of an SIS mixer is limited by the capacitance and series inductance of the junction(s) as described in [7]. To reduce the series inductance, we proposed a new low-inductance circuit for SIS mixers using series arrays of junctions; the junction capacitance can be reduced by using junctions with higher critical current density. Fig. 9 shows the layout of the main part of the RF circuit of the Band-8 mixer, and Fig. 10 shows the mixer connected to the RF/LO waveguide. The embedding impedances seen by each SIS junction are shown in Fig. 11. The measured noise temperature of one such mixer is plotted in Fig. 12.

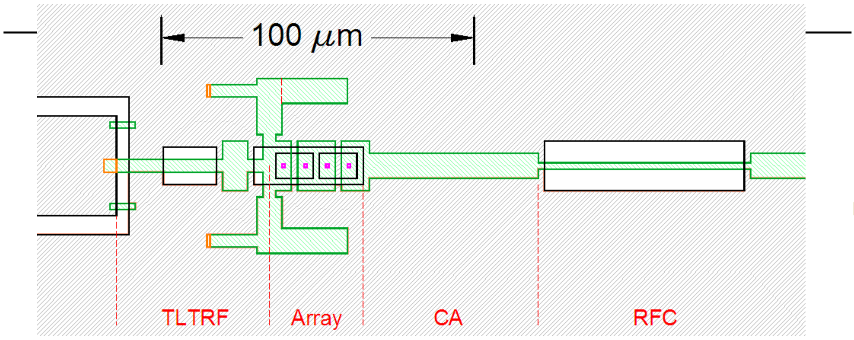


Fig. 9. The central part of the RF circuit of the Band-8 mixer. The coplanar waveguide on the left is connected to a waveguide probe. The Nb wiring layer (green) is separated from the Nb ground plane (gray) by an SiOx insulator layer. The four SIS junctions are cerise, and vias between the Nb layers are shown in orange.

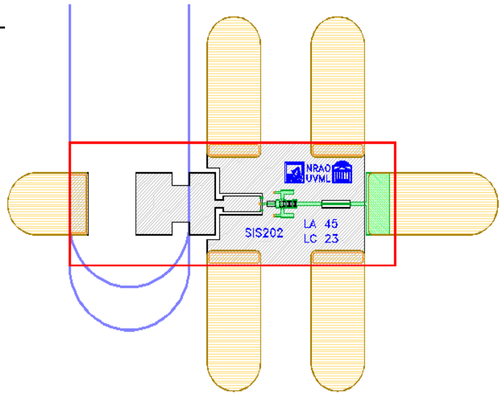


Fig. 10. The Si membrane mixer chip (red) coupled to the RF/LO waveguide.

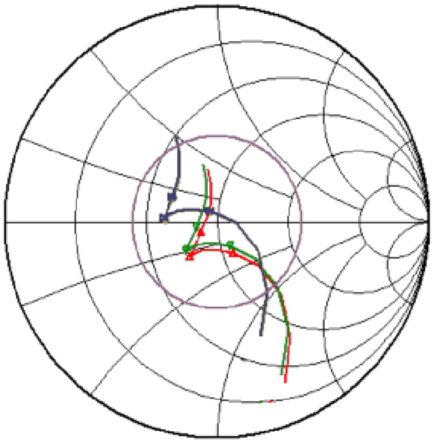


Fig. 11. Embedding impedance seen by the four SIS junctions (two of the curves overlap) from 340-540 GHz. Markers indicate the endpoints and center of ALMA Band 8. The Smith chart is normalized to the optimum source impedance. The purple circle is at |ρ| = 0.4.

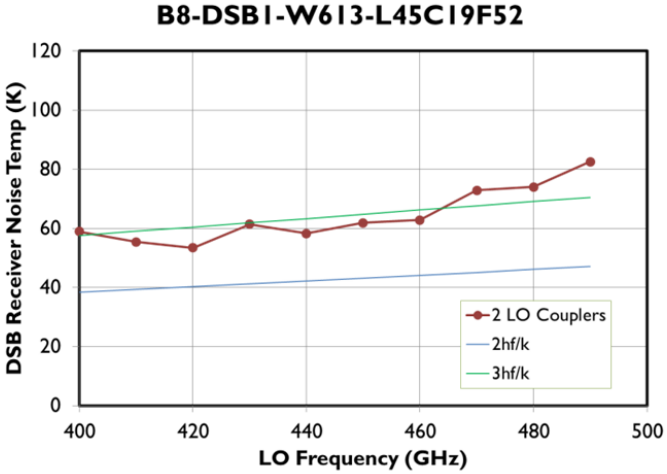


Fig. 12. Double sideband receiver noise temperature versus LO frequency for the Si membrane mixer when using two LO coupler modules (16 dB coupling).

The mixer design for Band 10 is similar in concept to the Band-8 design above. In order to keep the inductance of the series-connected SIS junctions sufficiently low to allow the required RF bandwidth, only two SIS junctions are used. Two designs have been developed, both using Nb/Al-AlN/NbTiN junctions, but one with Nb and NbTiN conductors in the tuning circuit and the other with normal metal (Al) conductors. Fig. 13 shows the RF tuning circuit. These circuits will be fabricated once the process for Nb/Al-AlN/NbTiN junctions is sufficiently developed to give reproducible mixers in the quantities required for ALMA.

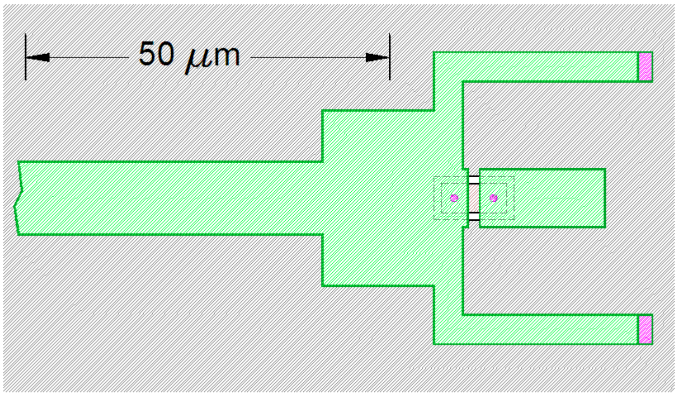


Fig. 13. RF tuning circuit of the Band-10 SIS mixer. The ground-plane (gray) is separated from the wiring layer (green) by an SiOx insulator layer. The red circles are the two SIS junctions. At the ends of the quarter-wave stubs, vias to the ground plane are shown in cerise. As in Fig. 9, the DC and IF connection is via a high-impedance RF choke circuit at the right (not shown), and a broadband waveguide probe is connected at the left.

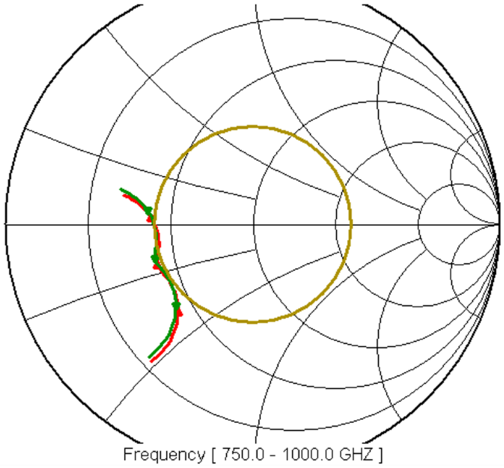


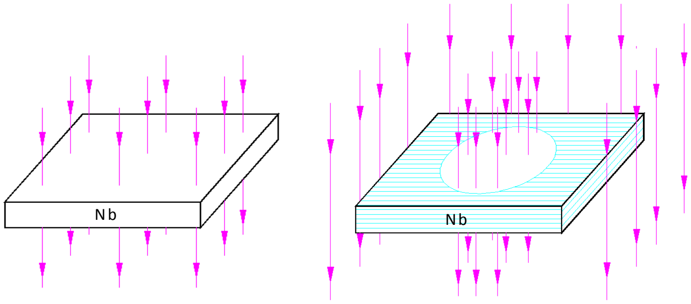
Fig. 14. Embedding impedance seen by the two SIS junctions from 750-1000 GHz. Markers indicate the endpoints and center of ALMA Band 10. The Smith chart is normalized to the optimum source impedance. The yellow circle is at |ρ| = 0.4.

2. Elimination of trapped flux

Trapped magnetic flux is a perennial problem with sub-mm wavelength SIS mixers. The ALMA receivers have a complex de-gaussing process which often fails on first attempt. Mixers with multiple SIS junctions are particularly prone to trapped flux difficulties because it is not possible to adjust the applied magnetic field to suppress the critical currents in all the junctions simultaneously if the different junctions see different amounts of trapped flux. In order to find a more consistent solution to the de-gaussing process, we have tried to understand the mechanism of flux trapping in superconducting circuits.

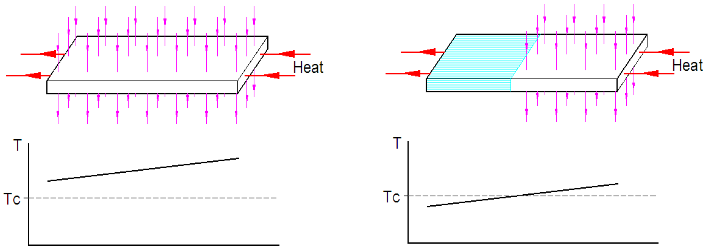
Magnetic fields are unavoidable in practical radio astronomy receiver dewars. They originate from ferrite isolators, residual flux in magnetic material, near-by motors, and the earth's field. When a superconductor is cooled through its critical temperature T_C, magnetic fields are excluded from the interior of the superconductor (the Meissner effect) by currents on the surface. In the ideal situation, the temperature is uniform throughout the superconductor during cooling, but in practice the interior of the superconductor may not cool as quickly as the perimeter; this could occur if the superconductor is a film on a substrate such as quartz.. If the superconductor is cooled down in the presence of a magnetic field in such a way that the edges become superconducting before the central region, the flux in the regions which have gone superconducting first is excluded, either being pushed outside the sample, or being pushed into the central region of the sample which has not yet gone superconducting. As cooling proceeds further, the central normal region must get smaller, but the flux trapped in it can not be pushed out. Our hypothesis is that when cooling is complete, the trapped flux has been squeezed into a small region where its intensity is great enough to increase the local critical temperature sufficiently to keep material in that small region normal. This is illustrated in Fig. 15 which shows a sample of superconductor above its critical temperature in the presence of a magnetic field (left diagram), and (right diagram) as the outer regions cool below T_C expelling the flux from the superconducting region and trapping a bunch of flux in the central region which remains above T_C.

Fig. 15. Superconductor in a magnetic field. Left: Above T_C. Right: Cooled from the edges, the blue region goes superconducting before the central region.

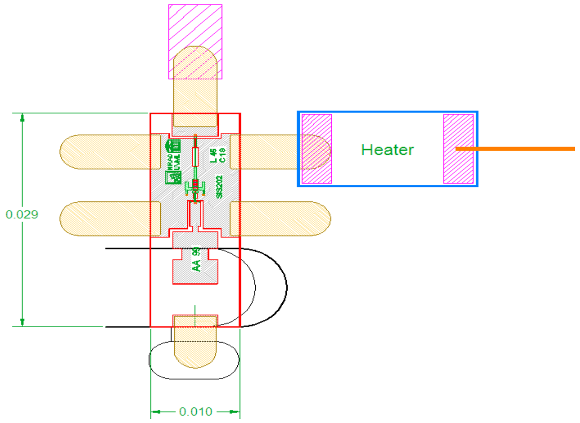


To prevent flux trapping in the superconductors as it is cooled, we consider a *gradient cooling* method, in which a temperature gradient is maintained across the sample as it is cooled below T_C. As depicted in Fig. 16, this allows magnetic flux to be squeezed out of the sample starting from one side, and avoids the situation shown in Fig. 15 in which, at some stage of the cooling process, there is a region of normal material completely surrounded by superconducting material.

Fig. 16. Cooling the sample from the left end produces a temperature gradient along the sample, so one end goes superconducting first and the magnetic flux is swept out of the conductor.



Beamlead mixer chips are cooled through their beamleads. To produce a temperature gradient along the mixer substrate we put a small chip resistor under one of the beamleads, as shown in Fig. 17, and heat it with a DC current.



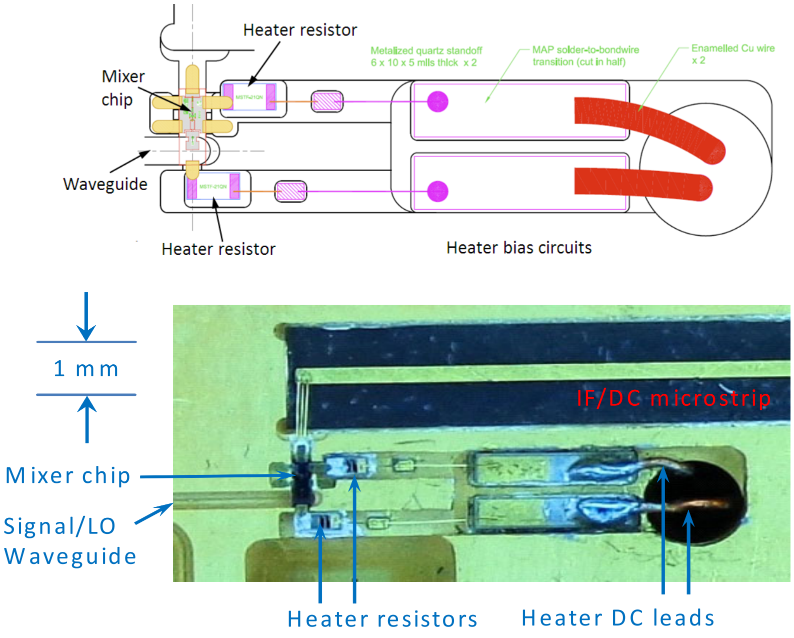


Fig. 17. Left: Band-8 beamlead mixer chip with a heater resistor. Right: A Band-8 beamlead mixer with two heater resistors, one under the top right beamlead, and the other under the bottom beamlead.

Example of trapped flux removal. The I(V) curves in Fig. 18 illustrate the trapped flux removal procedure on the Band-8 mixer in Fig. 17 (This mixer has one of the early beamlead and membrane chips with Nb/Al-AlN/Nb junctions, whose I(V) characteristics were not of the highest quality.) Initially, the iron magnet circuit was de-gaussed using the standard method of periodically varying the coil current between its positive and negative extremes, then gradually reducing the amplitude of the current variation to zero. At this point the I(V) curve of Fig. 18(a) was measured. Clearly one of the four junctions has enough magnetic field to suppress its critical current almost completely. The heater at the bottom of the mixer chip was then turned on for a few seconds until the mixer was above its critical temperature and looked like a resistor. The heater was then turned off gradually, and the I(V) curve of Fig. 18(b) was measured. Finally, the coil current was adjusted to 24 mA, at which point the critical currents of all four junctions were suppressed, as shown in Fig. 18(c).

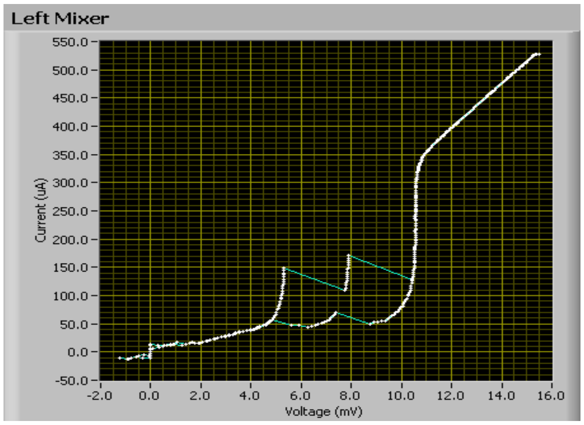


Fig. 18(a). Initial I(V). Imag = 0.

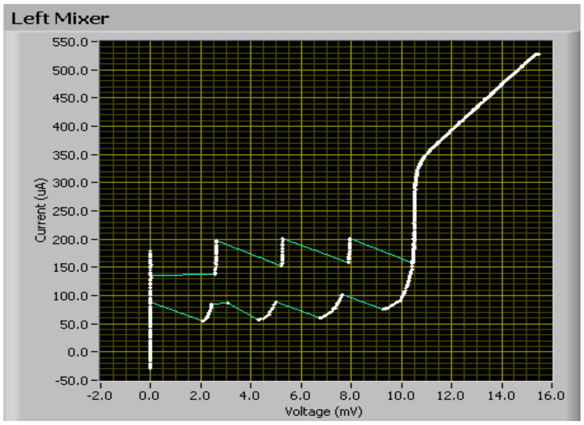


Fig. 18(b). Heater turned on then off. Imag = 0.

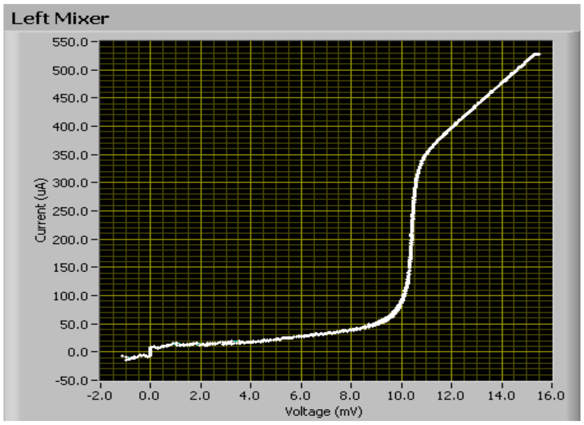


Fig. 18(c). Heater turned on, then off. Then Imag = 24 mA.

3. Sideband separating and balanced SIS mixers

Several configurations are possible for receivers using sideband-separating and balanced mixers. Sideband-separating mixers are used for ALMA Bands 3-8 as a means of reducing the atmospheric contribution to the system noise, but LO sideband noise also contributes a significant component to the system noise at some LO and intermediate frequencies, and this can potentially be reduced by using a balanced mixer configuration. The input characteristics of balanced and sideband-separating mixers with quadrature and 180° input hybrids are examined in the companion report on mixers for a second generation Band-6 mixer [7]. Like the balanced amplifier, balanced and sideband-separating mixers using a quadrature input hybrid are inherently well matched, which can help to reduce baseline ripples and, in SIS mixers, improve the image rejection.

The levels of the signals emerging from the input port at the image and LO frequencies are also important in some applications, as are the down-converted local oscillator sideband noise and the thermal noise contribution of the fourth-port termination on the input hybrid. These depend on the mixer configuration. These effects are considered for balanced and sideband-separating mixers of four basic types in [7].

4. Mixer-IF interface

The mixer-to-IF amplifier connection is critical for SIS mixers. To minimize interaction between the output of the mixer and the input of the IF amplifier, a ferrite isolator is desirable, but wideband cryogenic isolators are lossy and their physical size constrains the layout of an ALMA cartridge which must accommodate four such units for a dual-polarization receiver with sideband-separating mixers. A better alternative is to use balanced IF amplifiers which are now feasible using superconducting 90° hybrids. An IF hybrid for 4-12 GHz, 3 x 1 x 0.25 mm, is currently under development as described in the companion report on the development of a second-generation Band-6 receiver [8].

5. Conclusion

In this study, essential steps have been taken towards a next-generation SIS receiver for ALMA Band-10. Progress has been slower than planned, in part because of the loss of personnel in the mm receiver group who until recently could not be replaced, and in part because the engineering problems encountered were more difficult than anticipated. However, we are now in a good position to continue working towards the goal of a substantially improved front-end for Band 10 using the new mixer designs and procedures described here.

REFERENCES

[1] A. R. Kerr, S.-K. Pan, W. G. Lyons, "The Genesis of SIS Mixers – The Legacy of John Tucker in Radio Astronomy," 2015 IEEE International Microwave Symposium, invited paper, Special Tribute Session to Prof. John R. Tucker, 20 May 2015. http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7166809

[2] Y. Fujii, A. Gonzalez, M. Kroug, K. Kaneko, A. Miyachi, T. Yokoshima, K. Kuroiwa, H. Ogawa, K. Makise, Zhen Wang ; Y. Uzawa, "The First Six ALMA Band 10 Receivers," IEEE Trans. Terahertz Science and Technology, vol. 3 , no. 1, pp. 39-49, 2013. http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6423869

[3] M. E. Cyberey, D. Oakland, J. Z. Zhang, A. R. Kerr, S.-K. Pan, and A. Lichtenberger, "Optical Spectroscopic Analysis of ICP Nitridation for SIS Junctions with AlN Barriers," IEEE Transactions on Applied Superconductivity, Vol PP, issue 99 2015. http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7003996

[4] Engineered Components & Packaging http://www.ecpplastictrays.com/Pages/50CavityNumberedTray.aspx

[5] Dick Blick Art Materials, http://www.dickblick.com/search/?q=round+0+brush&x=0&y=0&sp_cs=UTF-8&page=1&restrictBy=brand%3ABlick&maxResults=96

[6] A. R. Kerr, S.-K. Pan, S. M. X. Claude, P. Dindo, A. W. Lichtenberger, J. E. Effland and E. F. Lauria, "Development of the ALMA-North America Sideband-Separating SIS Mixers," IEEE Trans. Terahertz Science and Technology, v. 4, no. 2, pp. 201-212, Mar 2014. http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6740089

[7] A. R. Kerr, "Some fundamental and practical limits on broadband matching to capacitive devices, and the implications for SIS mixer design," IEEE Trans. Microwave Theory Tech., vol. MTT-43, no. 1, pp. 2-13, Jan. 1995. http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=363015

[8] A. R. Kerr, J. Effland, and J. Mangum, " Towards a Second Generation SIS Receiver for ALMA Band 6," a companion report on ALMA development work, submitted March 2016.