VLBA Sensitivity Upgrade Memo 36

ESSR Acceptance Plan

Walter Brisken

June 29, 2011

Abstract This document describes the immediately forseen usage cases for the X-Cube Ethernet Software Switch Recorder (ESSR) and the test criteria by which acceptance will be determine.

1 Introduction

The use cases described in this document are expected to be used in VLBA operations in the next 12 months. The criteria used to evaluate the ESSR for usability include ability to configure desired modes and correct operation. The specified tests aim to be reasonably complete while still not onerous. We aim to complete the evaluation of the ESSR within one month of delivery. The current estimated delivery date of the first articles is July 19, 2011.

2 Use cases

There are four use cases, illustrated in Fig. 1, which are expected to be used in the near term. In all four cases a simple mapping betweein input ports and output ports can fully describe the required behavior; no introspection of the data is required for packet routing. Each use case is shown in the figure with a particular choice of input and output ports to be used. Acceptance will require that all configurations defined by interchange of input and/or output ports also work. The four use cases are:

1. **Single passthru** A mode where one RDBE generates data and one Mark5C is to record it. There are 4 possible configurations when considering the two choices for input and the two choices for output. In this mode, no data can be dropped and packet order needs to be maintained.

2. **Splice 2 to 1** A mode where data is generated by two RDBEs and recorded by one Mark5C unit. It is required that the order of packets from each input is preserved. The relative order of packets received simultaneously from the two inputs is not important. No data can be dropped. There are two configurations available by choice of the output port. These will be designated $0 + 1 \rightarrow 0$ and $0 + 1 \rightarrow 1$.

3. **Dual passthru** In this mode two RDBEs generate data, each being recorded by one specified recorder. There are two configurations: $0 \rightarrow 0$ & $1 \rightarrow 1$, and $0 \rightarrow 1$ & $1 \rightarrow 0$.

4. **Duplicate input** In this mode the data coming from one input port is directed to both outputs. There are two possible configurations, $0 \rightarrow 0 + 1$ and $1 \rightarrow 0 + 1$.

Overall, there are 10 different configurations to be tested.

There is an additional use case which has been discussed in the past and may have long term value. In this mode individual packets received from one or two RDBEs are inspected to determine the destination Mark5C rather than relying on a fixed mapping between input and output ports. This use case will be untestable and unusable until multi-thread VDIF data can be produced by RDBEs; this class of modes is not included in the acceptance criteria and won't be discussed further in this document.

3 Acceptance metrics

Due to constraints of test setups that can be realized on the required timescale, the level of scrutiny that can be given to each mode of operation is not uniform. The acceptance tests in all cases will use RDBEs

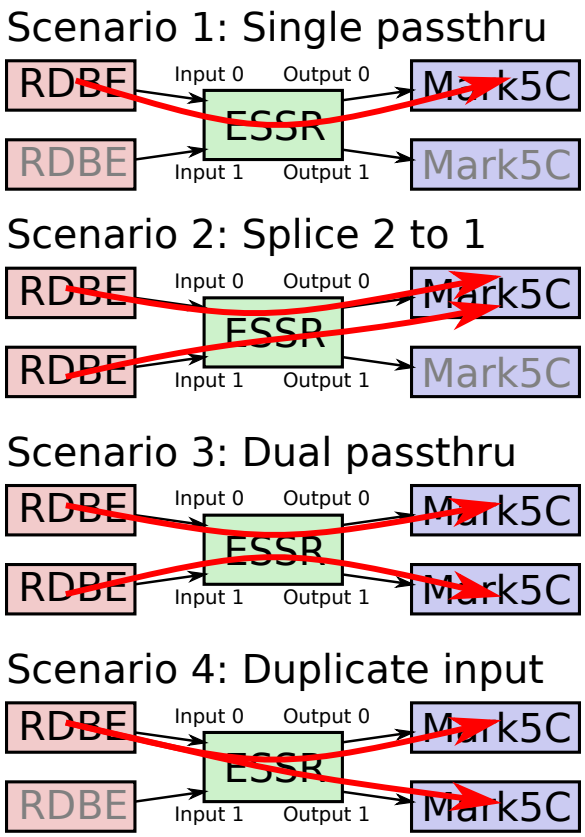

Figure 1: *ESSR use cases.* Four topologically unique use cases are expected to be required in the near future. Variants of each with input and/or output ports swapped should be considered required as well. See text for descriptions of each. Connectivity between each unit is via point-to-point 10 Gbit ethernet links; traffic on these interfaces is unidirectional. Each device will be controlled via a separate 1 Gbit ethernet interface.

as sources of data. Current FGPA code available for the RDBE produces a limited subset of data product types. Only Mark5B format data will be produced and data rates will be restricted to 2048 Mbps with the PFB personality and 1024 Mbps with the DDC personality.

The following metrics will be used:

1. **Data correctness** The data frames will be examined for the correct order of arrival at the Mark5C unit(s) and, to the degree possible, the data contained within the packets will be examined for plausibility.

2. **Path correctness** In all cases both Mark5C units attached to the ESSR will be set to record. Each Mark5C unit receiving will be examined to determine if it came from the expected source or that it received no data in cases where that unit was not selected.

3. **Data completeness** The RDBE data sources can robustly be programmed to deliver a specified number of data packets. The quanity of data recorded on the Mark5C unit(s) will be compared against the expected data volume.

Existing tools from the DiFX development will be used to evaluate the data. Specifically, the `m5d` program will be used to validate the data format and examine timestamps and `m5spec` will be used to determine the

plausibility of the formatted data. In the case of the "dual passthru" and "duplicate input" use cases, a zero baseline correlation using `zerocorr` will be performed. In order to minimize the testing effort, at most one configuration for each use case will be tested for data correctness unless problems are found.

4 Acceptance tests

4.1 Practical tests

The following tests will be done to ensure the device is aligned with our operating needs:

1. **Power-up** The unit when turned on (and when power is restored after an outage) should automatically boot the operating system, load any required device drivers, and start the soft switch software.
   Pass/Fail: _____ Comments: _____

2. **Up-time test** The unit when operating in soft switch mode should be stable, without unbounded memory use growth, for a period of 1 week.
   Start date/time: _____ Memory used: _____
   Stop date/time: _____ Memory used: _____
   Pass/Fail: _____ Comments: _____

4.2 Use case tests

The table below explicitly lists the tests to be performed for acceptance. In all cases the data rate refers to that being produced by each RDBE.

Test	Configuration	Data rate (Mbps)	Metric	Pass/Fail	Comments
3	$0 \rightarrow 0$	2048	Data correctness		
4	$0 \rightarrow 0$	2048	Path correctness		
5	$0 \rightarrow 0$	2048	Data completeness		
6	$0 \rightarrow 1$	2048	Path correctness		
7	$0 \rightarrow 1$	2048	Data completeness		
8	$1 \rightarrow 0$	2048	Path correctness		
9	$1 \rightarrow 0$	2048	Data completeness		
10	$1 \rightarrow 1$	2048	Path correctness		
11	$1 \rightarrow 1$	2048	Data completeness		
12	$0 + 1 \rightarrow 0$	1024	Path correctness		
13	$0 + 1 \rightarrow 0$	1024	Data completeness		
14	$0 + 1 \rightarrow 1$	1024	Path correctness		
15	$0 + 1 \rightarrow 1$	1024	Data completeness		
16	$0 \rightarrow 0$ & $1 \rightarrow 1$	2048	Data correctness		
17	$0 \rightarrow 0$ & $1 \rightarrow 1$	2048	Path correctness		
18	$0 \rightarrow 0$ & $1 \rightarrow 1$	2048	Data completeness		
19	$0 \rightarrow 1$ & $1 \rightarrow 0$	2048	Path correctness		
20	$0 \rightarrow 1$ & $1 \rightarrow 0$	2048	Data completeness		
21	$0 \rightarrow 0 + 1$	2048	Data correctness		
22	$0 \rightarrow 0 + 1$	2048	Path correctness		
23	$0 \rightarrow 0 + 1$	2048	Data completeness		
24	$1 \rightarrow 0 + 1$	2048	Path correctness		
25	$1 \rightarrow 0 + 1$	2048	Data completeness		