

Correlator electronics

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List of hardware elements to be discussed

- Correlator Interface Cards (**CI**)
- Correlator Cards (**CC**)
- Long Term Accumulator (**LTA**)
- Final Adder (**FA**)
- Data Port Interface (**DPI**)

Topics to be discussed

- Hardware structure.
- Adder tree.
- Data rates.
- How the correlator results are output.
- Sub-arrays.
- Binning (for side-band separation)
- Time stamp and padding.
- CAN monitor and commands.
- How the LTA card is setup.
- 2-antenna correlator.
- APP (**ALMA Phasing Project**) infrastructure.

Hardware structure

The IF (Intermediate frequency) is split into 4 basebands with signals of 2GHz bandwidth per baseband.

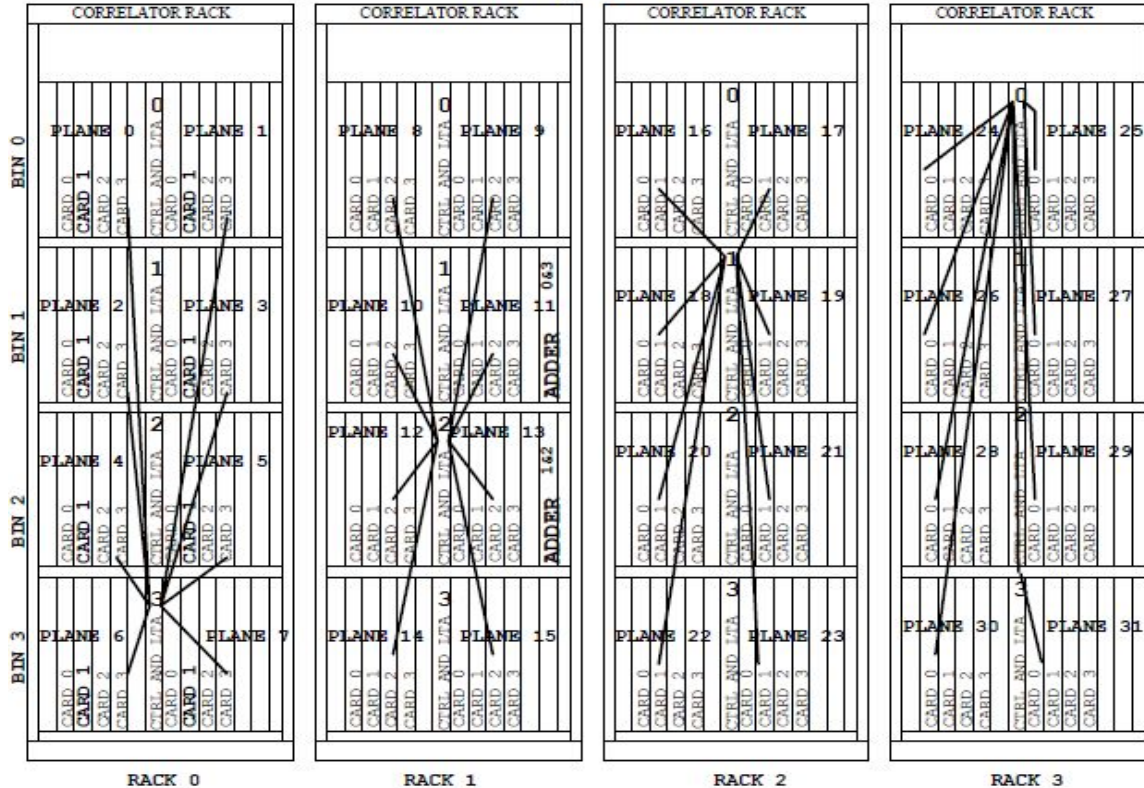
The BL correlator is composed of 4 quadrants, each one processes one base band pair (Pair because is composed by both orthogonal polarizations)

Each quadrant contains (correlator electronics):

- 16 LTAs (**L**ong **T**erm **A**ccumulator)
- 2 FAs (**F**inal **A**dder)
- 4 DPI (**D**ata **P**ort **I**nterface)
- 128 CC (**C**orrelator **C**ards)
- 128 CI (**C**orrelator **I**nterface)

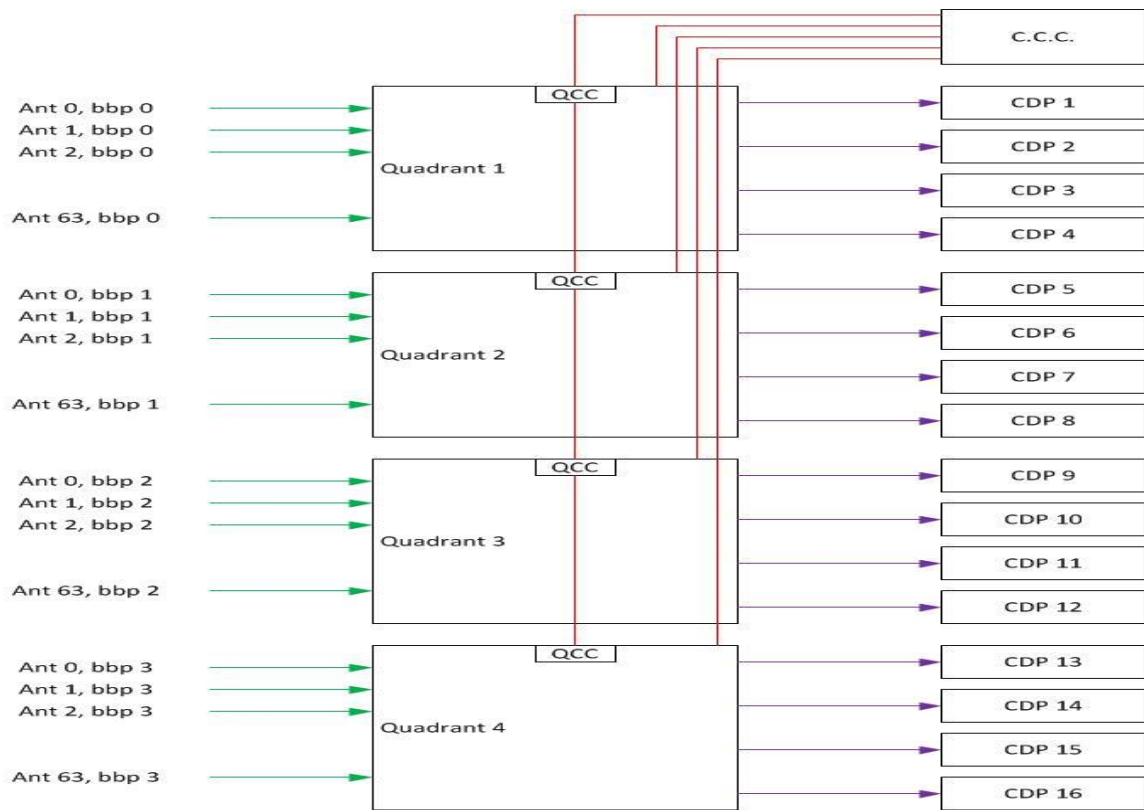
Hardware structure (C.C. to L.T.A.)

ONE QUADRANT



- LTA is connected to the CCC.
- The LTA generate and provide the control words to the CC.
- One LTA process the data produced by 8 CC.
- LTA is also the interface between CCC and CC

Hardware structure (correlator side)



Correlator as a “black box”

Inputs: digitized signals (via FO connection, custom protocol)

64 inputs (64 antennas)

$4\text{bbp} \times 2\text{pol.} \times 3\text{bits} \times 4\text{GS/s} = 96\text{Gb/s}$


input/output: CAN bus (monitor and control)

5 channels are used: 1 per quadrant (LTA/SCC/DPI/FA/PIC) + 1 for all QCC

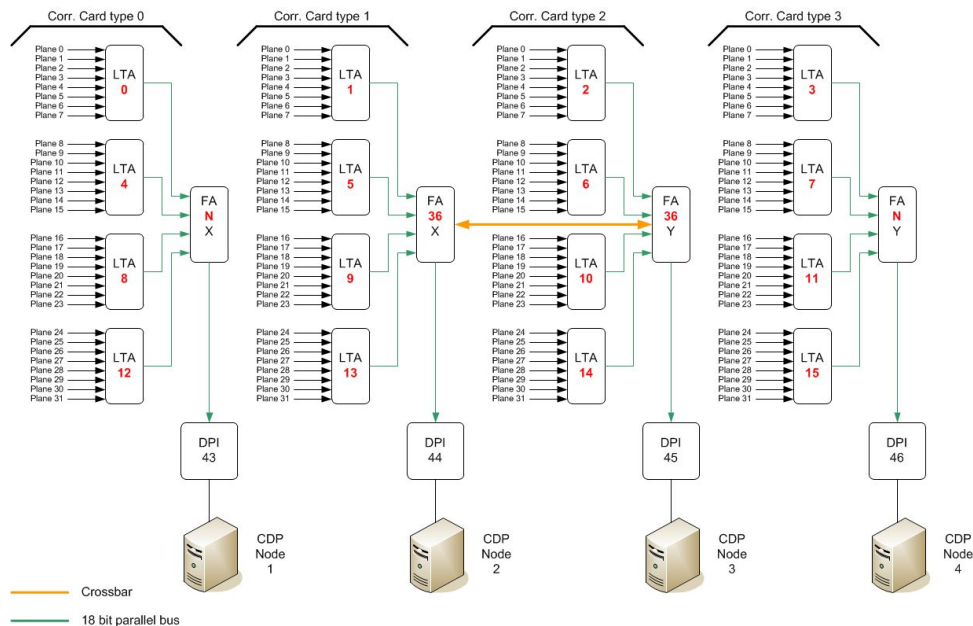
Output: raw correlation function (lag domain)

Highest data rate => 262144 lags / 16msec per DPI

1 Gbyte / second

-  Fiber Optic, 3 bits, 2 pol, 4GS/s
-  32 bits parallel bus, max 262144 lags/16msec
-  CAN bus

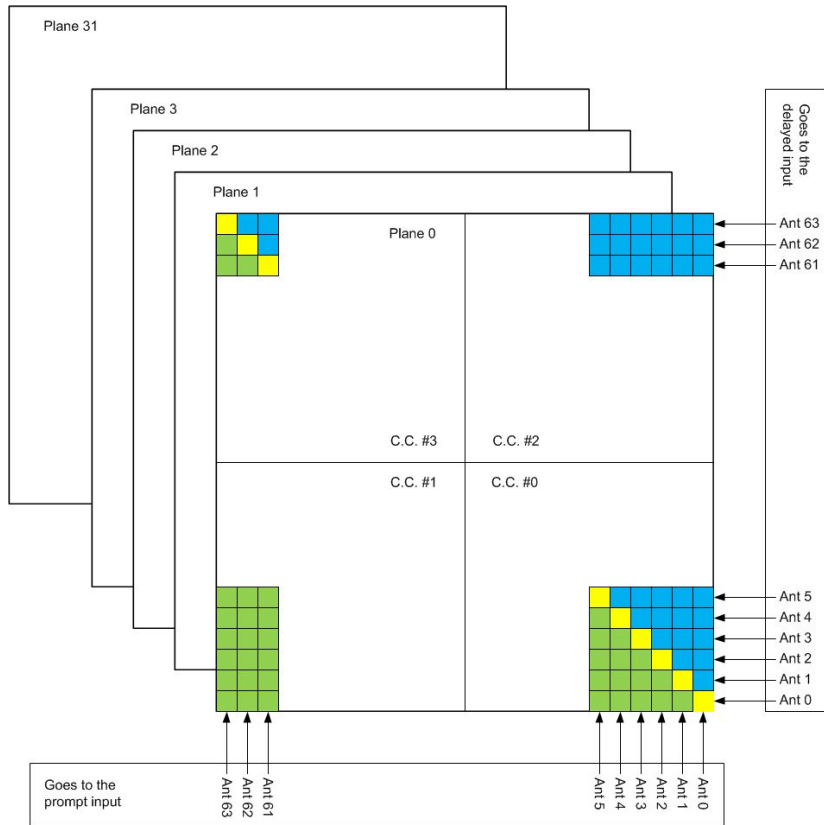
Hardware structure (connection diagram)



Quadrant	N
1	35
2	37
3	39
4	41

- 64 antennas => 2016 baselines
- CDP nodes 1 and 4 process the auto-correlation.
- CDP nodes 2 and 4 needs to have the auto-correlation data for normalizing the correlation function.
-

Hardware structure (detailed description of a “plane”)



- A “plane” can be regarded as a 64 x 64 matrix in which each element is a set of 256 lags values.
- One quadrant is made of 32 “planes”.
- One plane is made by 4 correlator cards.
- Planes can be added (TDM) or concatenated (FDM)
- Depending on the observation mode (TDM or FDM) a plane processes a time or frequency slice.

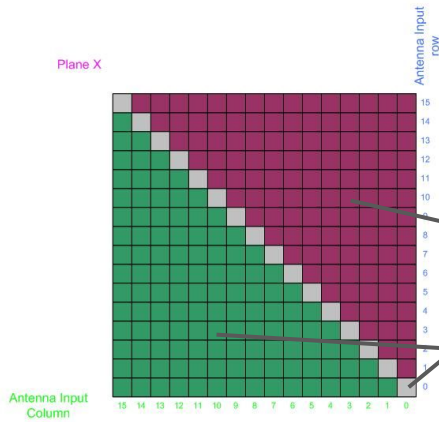
Hardware structure (how a correlation function is made)

- Auto-correlation

- Key property => $R_{xx}(t) = R_{xx}(-t)$
- Auto-correlation is made by the interactions from the diagonal

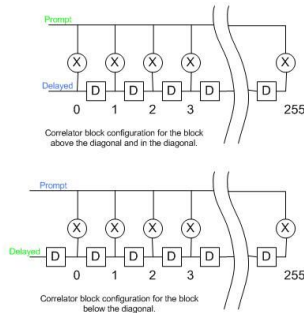
- Cross-correlation

- Key Property => $R_{xy}(t) = R_{yx}(-t)$
- $R_{xy}(t)$ for $t \in \{-N$ to $N-1\}$
- $R_{xy}(t)$ for $t \geq 0$
- $R_{yx}(t)$ for $t < 0$

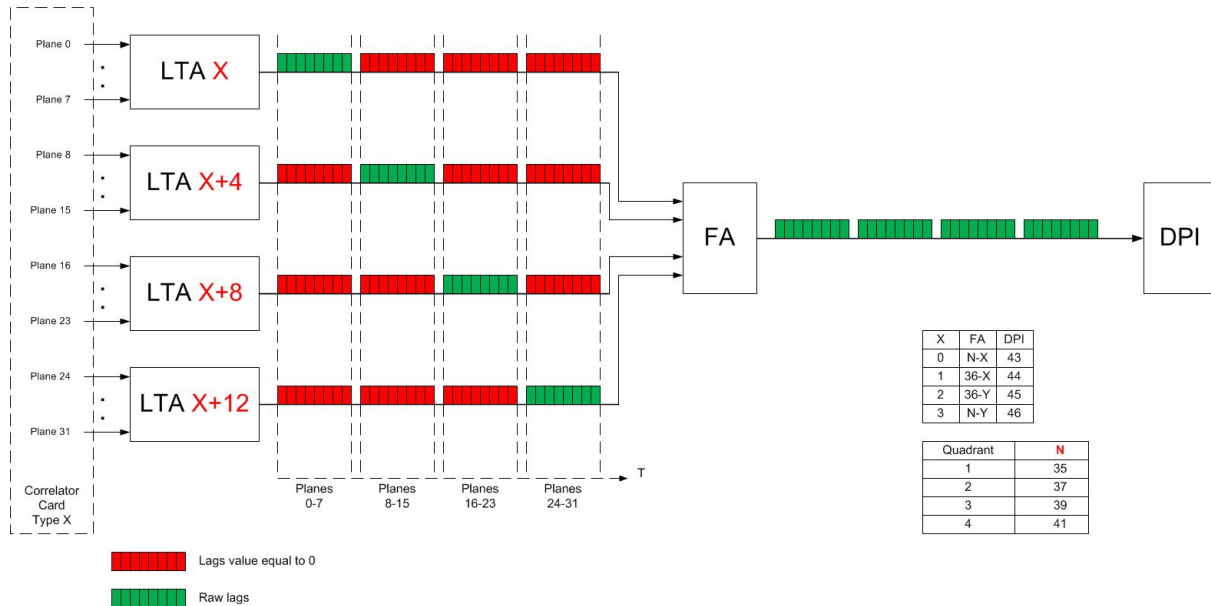


Each box represent an intersection of the correlator Matrix. Each intersection represents a 256 lags correlator block

- Leads, below the diagonal
- diagonal
- Lags, below the diagonal

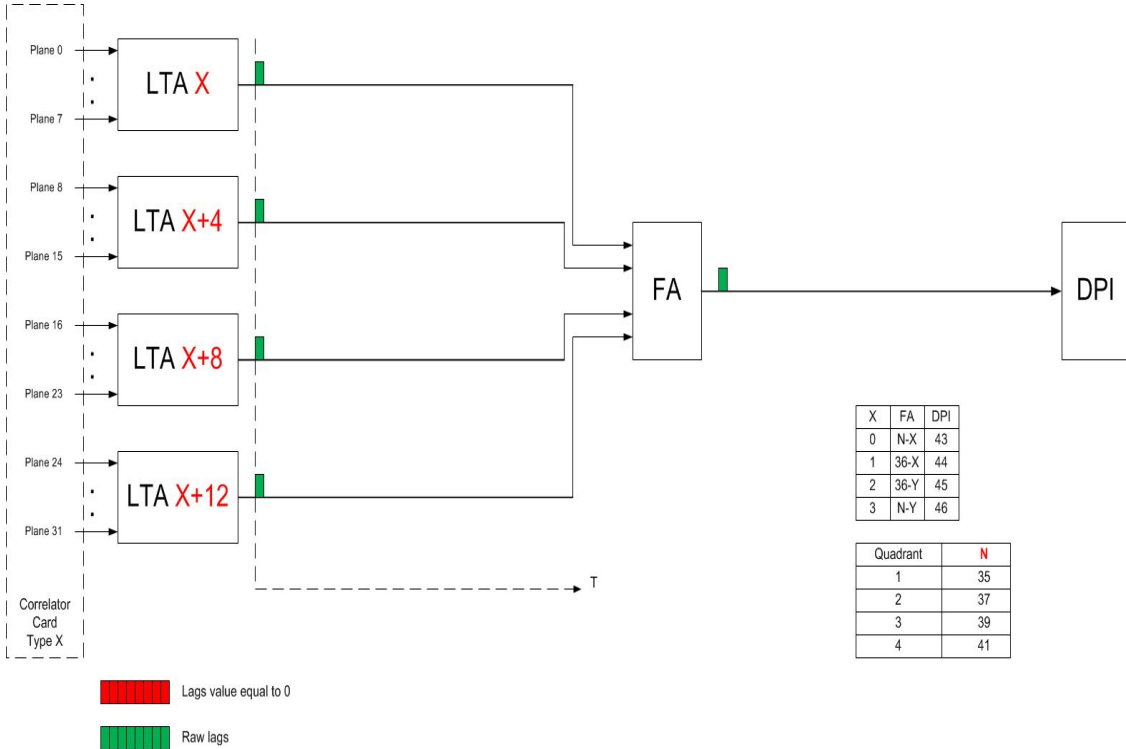


Adder tree (FDM case)



- Each LTA process 8 planes.
- Planes are added within the Final Adder
- The “planes” are concatenated.
- Groups of planes process different spectral regions

Adder tree (TDM case)



X	FA	DPI
0	N-X	43
1	36-X	44
2	36-Y	45
3	N-Y	46

Quadrant	N
1	35
2	37
3	39
4	41

- Each plane process different time chunks.
- In each LTA 8 time chunks are added.
- The addition of 32 planes is done by the FA.
- Bandwidth usage is 32 times lower than the FDM case.

Data rates

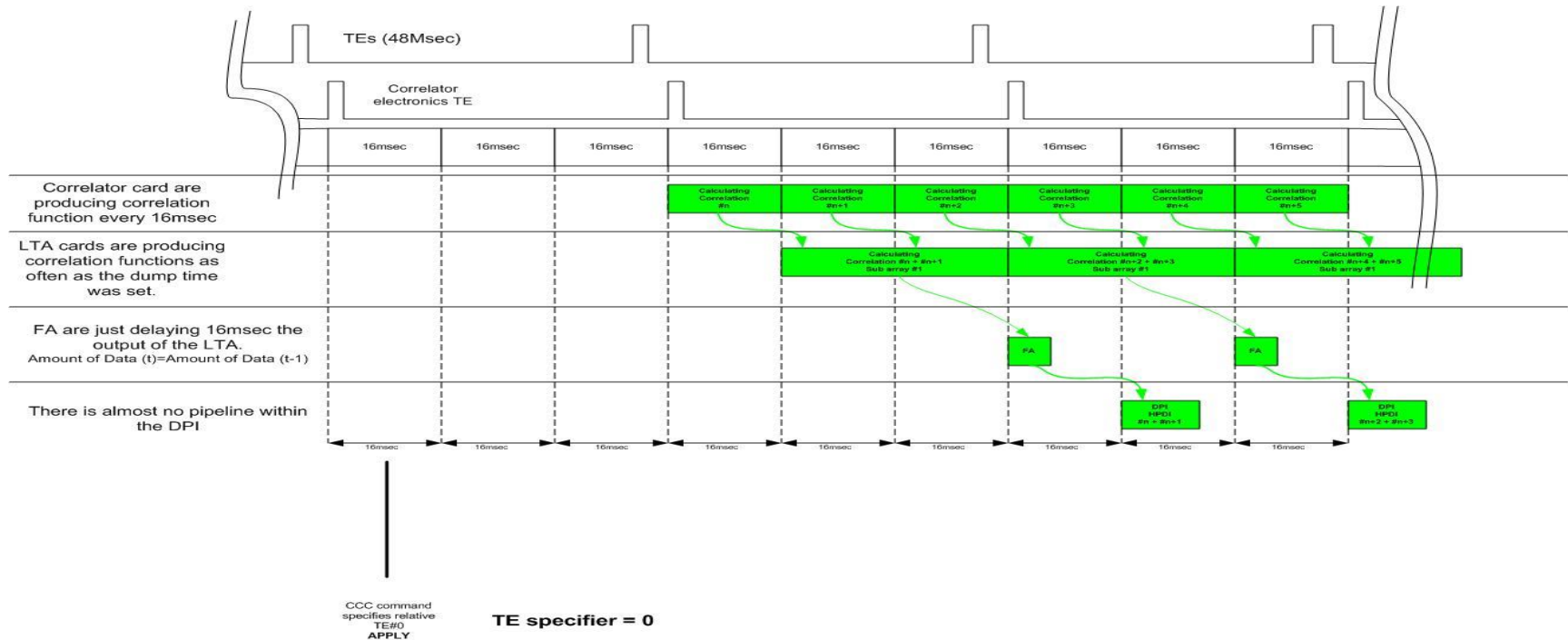
Data rate depends on:

- Observation modes (TDM/FDM)
 - FDM produces 32 times more data than TDM
- Dump rate
 - The minimal dump rate is 16 msec (including 1msec integration times)
 - The maximal amount of data (lags => 32 bits unsigned integer) is 262144/16msec per DPI
- Binning mode
 - Increases 3 times the bandwidth usage.
- Active sub-arrays
 - The total amount of data produced by the active sub-arrays must be equal to or below the bandwidth limit (262144 lags / 16msec)

From the point of view of a particular CDP node the data rate also depends of the set of active antennas.

How the correlator results are output (time)

- The time diagram below shows when the data is output upon the reception of an “apply” command.

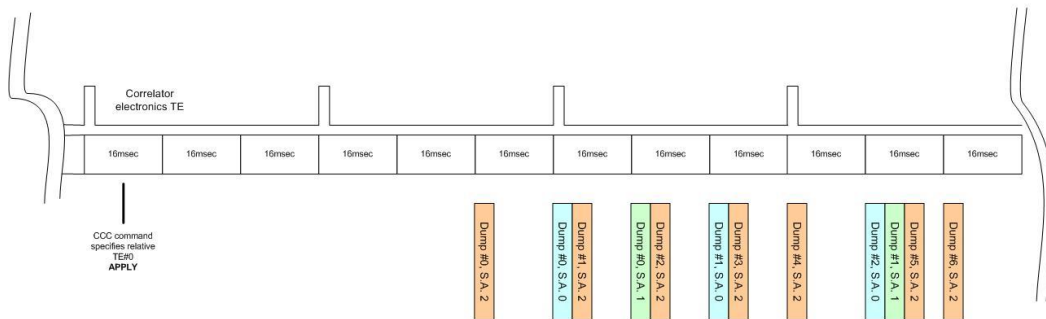
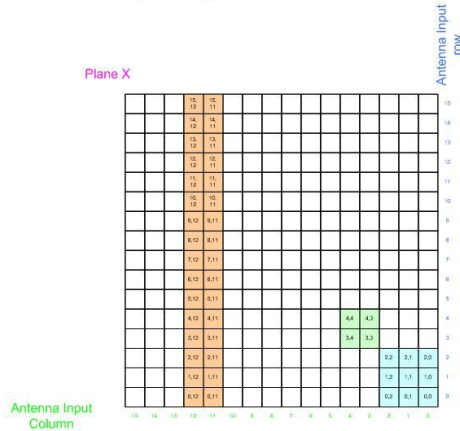
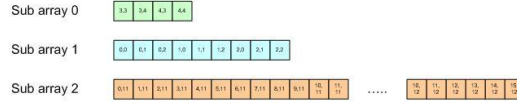


How the correlator results are output (sub-arrays)

Sub array 0: CAI_MASK=0x0018, mode 1, accum. Time= 2 tics

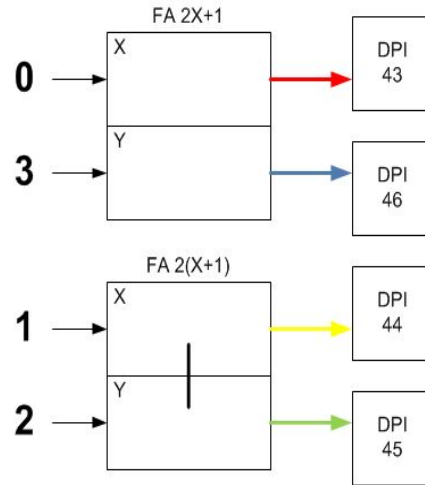
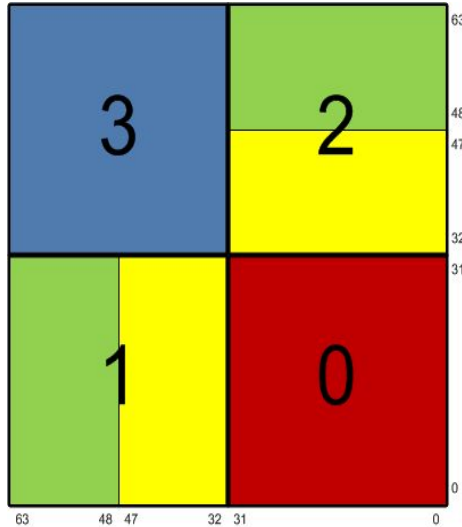
Sub array 1: CAI_MASK=0x0003, mode 71, accum. Time= 3 tics

Sub array 2: CAI_MASK=0x1800, mode 70, accum. Time= 1 msec



- Sub-arrays must share the available DPI-HPDI bandwidth.
- They are output following the configuration ID.
- More than one sub-array's results can begin output during a 16msec time slot.
- “Brown” array is a 1msec, only auto-correlation

How the correlator results are output (crossbar)



- The aim of the crossbar operation is to provide the “leads” and the “lags” for a given interaction.
- Crossbar introduces 16msec latency.

Sub-arrays

- The BL correlator hardware is able to run up to 16 independent arrays (the current ALMA hardware supports only 6, and currently the software only supports 4).
- The active arrays must be made of sets of antennas with no common elements.
 - The arrays configuration must be downloaded first (***download*** command)
 - The configuration words must be made based on which arrays are going to be active (***generate*** command)
 - The configuration words must be applied (***apply*** command)

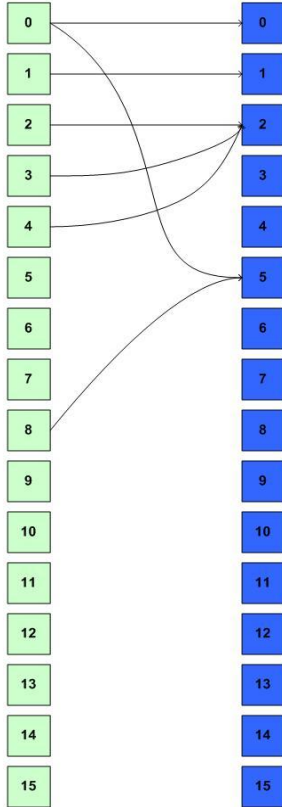
Sub-arrays (terminology)

Storage for up to 16 sets of configuration Parameters, typically each one Associated with a "sub array"

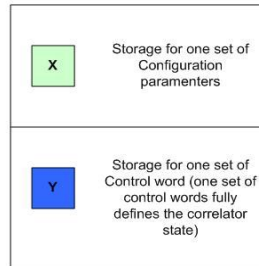
Configuration parameters Are downloaded from the CCC

One set of configuration Parameters downloaded to Specified storage location (one of 0-15)

One set of control words depends of the sub arrays used to generate it.



Storage for up to 16 sets of "control words" where one set fully defines the "state" of the correlator



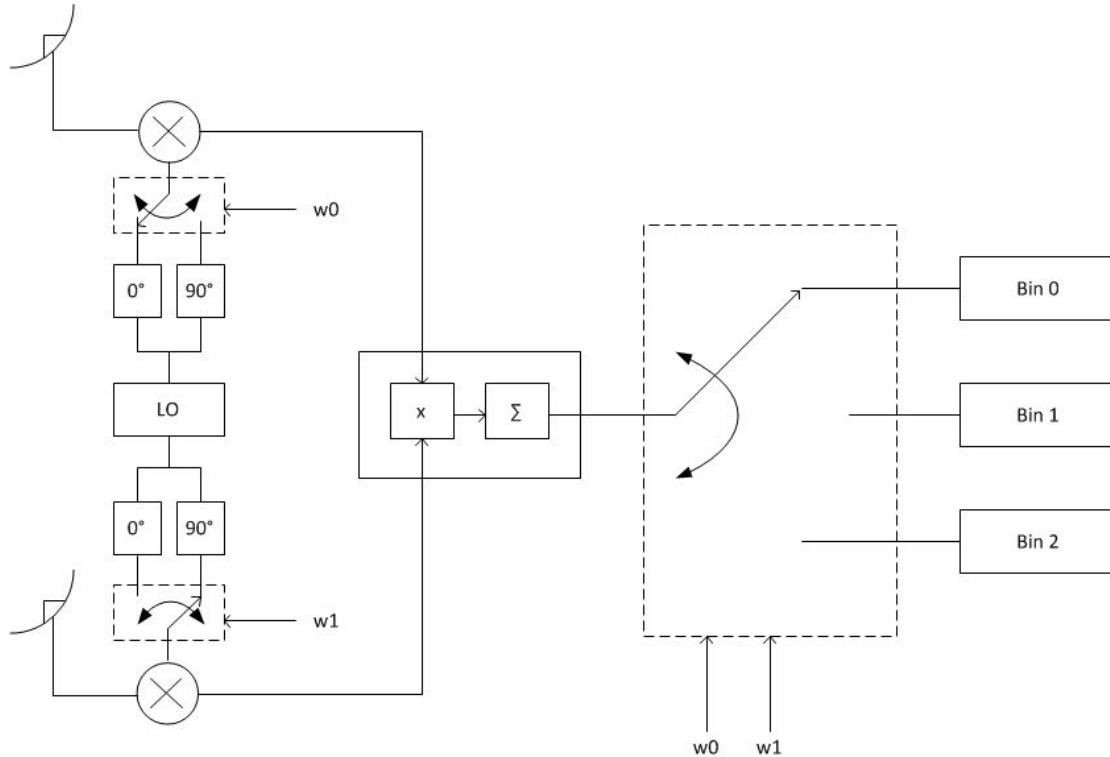
Configuration parameters: defines the set of antennas to be part of the sub array (CAI MASK), the observation mode, integration time etc

Correlator state: correlator state defines what the correlator hardware is actually doing. There is just one correlator state running at a given time.

Binning (for side-band separation)

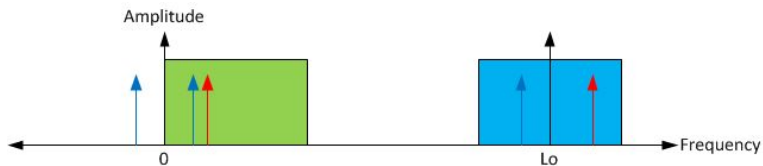
- The BL correlator is able to accumulate in different bins depending on the current Walsh state of each active antenna.
- The Binning for side-band separation allows to get the Upper and Lower side-band from the **cross-correlation** only (there is no support for performing this process in auto-correlation)
- Needed for dual side-band receivers (Band 9 and 10)
- It will be also handy for other bands (Dual Side Band)
 - According to the ALMA spec the rejection between sideband must be better than 10db (10%)

Binning principle



- 90-degree phase shift added by FLOOG in each antennas
- Modulated by Walsh sequence
- Depending on the Walsh state of two antennas, accumulate in one of three bins

Binning principle



BIN	Fsky	Fif	
0			
1			
2			

$$LSB = bin0 + D(bin1) - D(bin2)$$

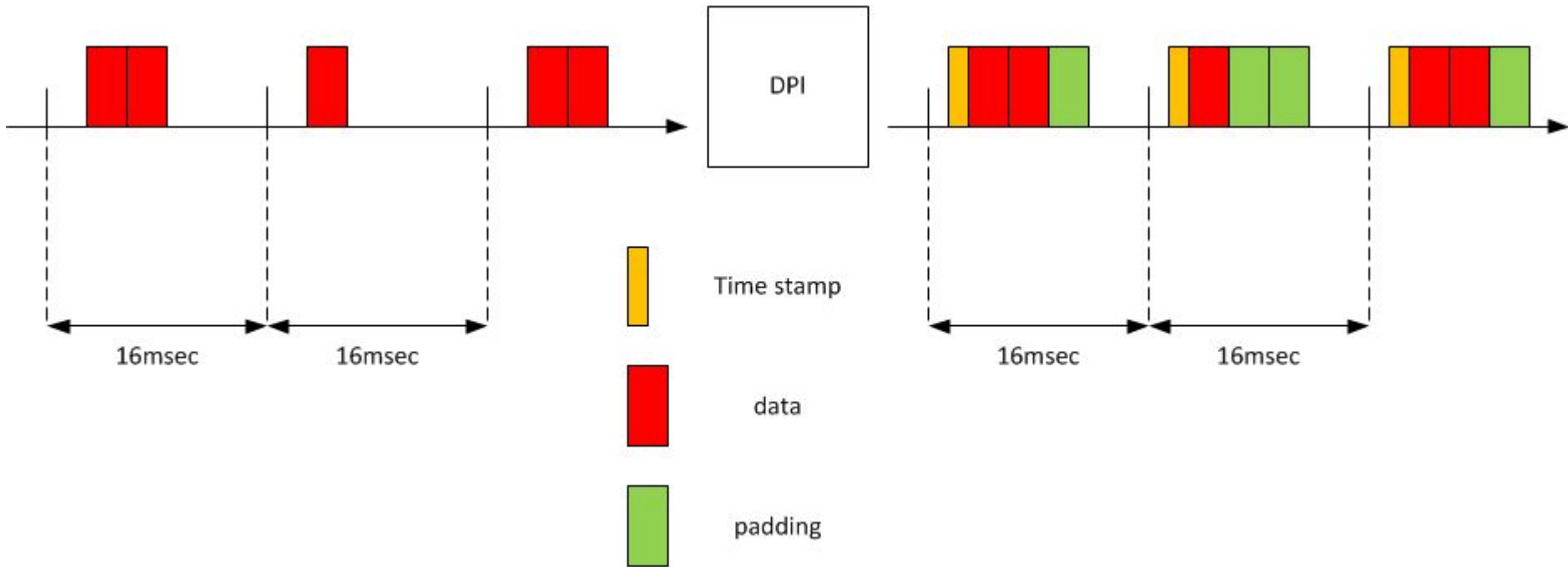
$$USB = bin0 - D(bin1) + D(bin2)$$

- Key property: $f(w)=c(f(-w))$
- The phase value is phase difference between antennas.
- 0 and 0 is the same as 90 and 90.
- Side-band separation only work for the cross-correlation.

Time stamp and padding

- For removing the RTAI (real time) component from the CDP nodes, the correlator hardware also provides (as a header) time information for each set of results.
- The header is made by a unsigned integer which is increased 1 unit every 16msec
- The DPI is the responsible unit to add the “time stamps” to the output stream.
- Time stamp is just a 32 bits counter
- Padding => fills with zeroes the unused bandwidth => the hardware always dumps 262144 lags every 16msec per DPI (zero is an impossible lag result)

Time stamp and padding



CAN monitor and commands (DPI)

- `Apply_time_date`
 - CCC issues a CAN broadcast command telling what will be the UTC time at next TE.
- `Set time-stamp and padding`
 - The time-stamp and padding can be individually enabled/disabled.
 - Backwards compatible

CAN monitor and commands (FA)

- Apply_time_date
 - CCC issues a CAN broadcast command telling what will be the UTC time at next TE.
- Send quadrant
 - Each quadrant has 2 Final Adders, the node ID changes as the quadrants changes.
 - The Final Adder broadcasts the quadrant number to all the control cards sharing the same CAN bus

Quadrant	FA (no crossbar)	FA Y (crossbar)
1	36	35
2	36	37
3	36	39
4	36	41

CAN monitor and commands (LTA)

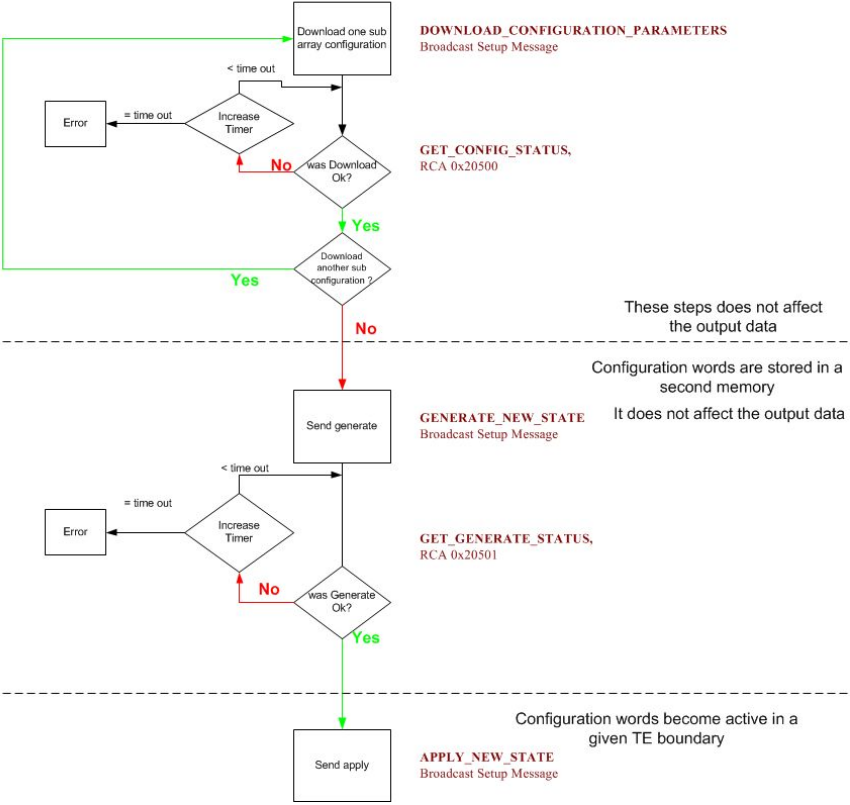
- Broadcast Command Messages
 - Download_Configuration_Parameters (data structure transfer)
 - Download_antenna_sum_mask (data structure transfer)
 - Download_90Degree_Sequences (data structure transfer)
 - Generate_New_State
 - Apply_New_State
 - SET_CIC_SUM_INPUT_SWITCH
 - Download_sum_scaling_data
 - Set_analog_sum_mode
 - Apply_Time_date
- Monitor points
 - GET_CONFIG_STATUS
 - GET_GENERATE_STATUS

CAN monitor and commands (PIC)

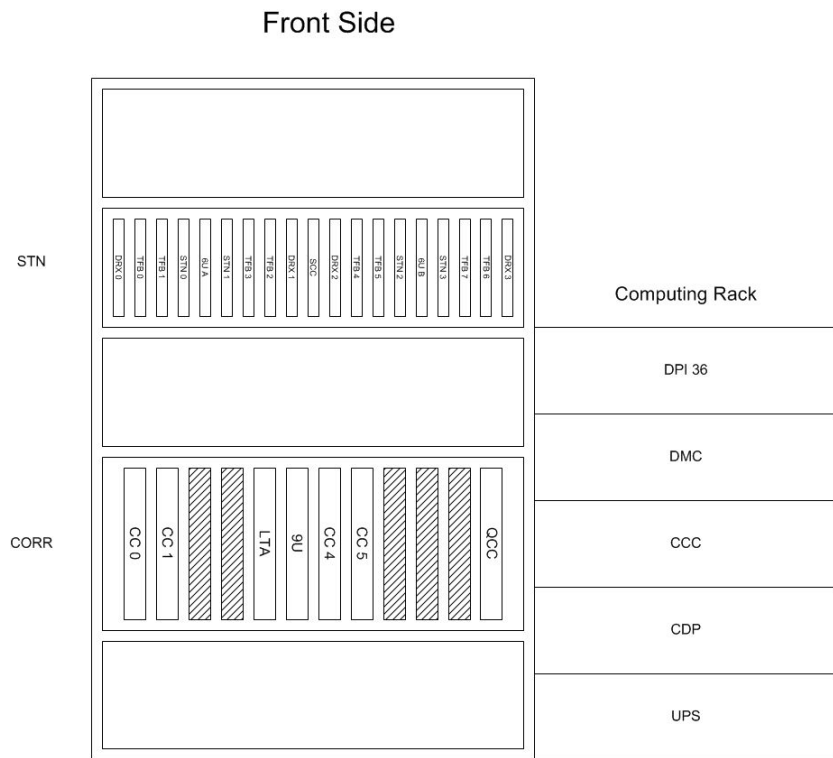
- Broadcast Command Messages
 - Apply_time_date
 - Download_VDIF_Header (data structure transfer)
 - SET_Pic_Control
- Monitor points
 - Get_Pic_Status (data structure)
 - Get_Te_Dll_Error_Status
 - Get_Download_Vdif_Header

How the control cards are setup (LTA)

LTA setup steps



2-antenna correlator

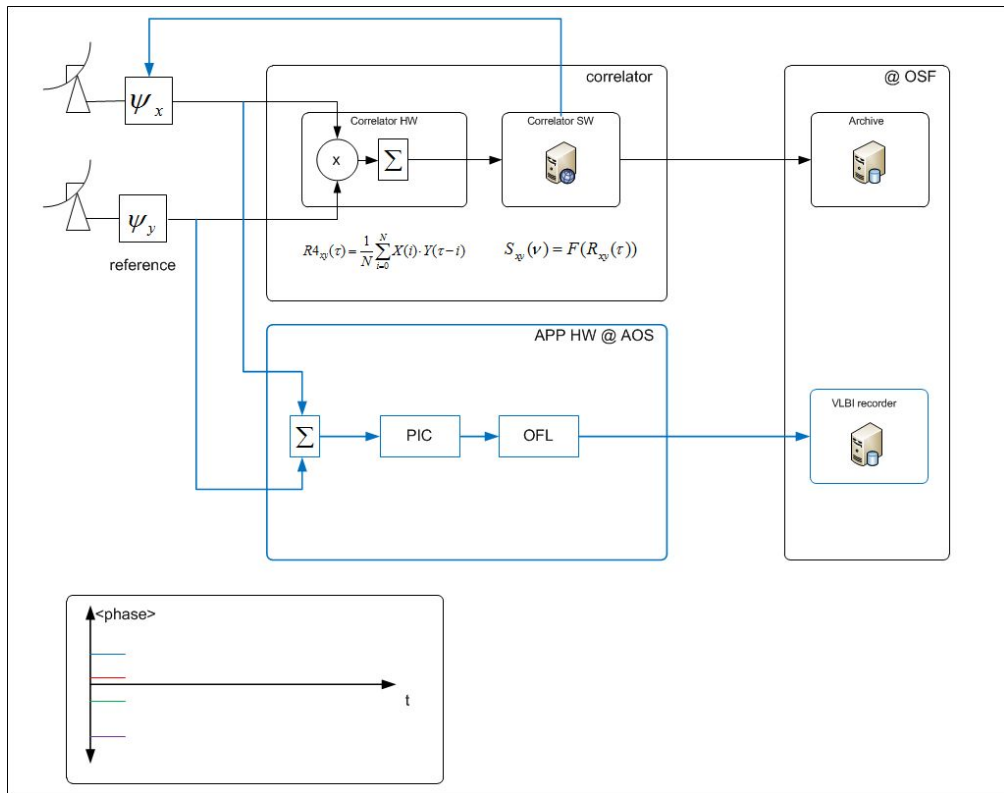


- Input for 2 antennas.
- 2 BBP
- Station electronics uses the same firmware as the BL correlator
- Correlator electronics runs a custom firmware
- It does not support sub-arrays
- No Final Adder

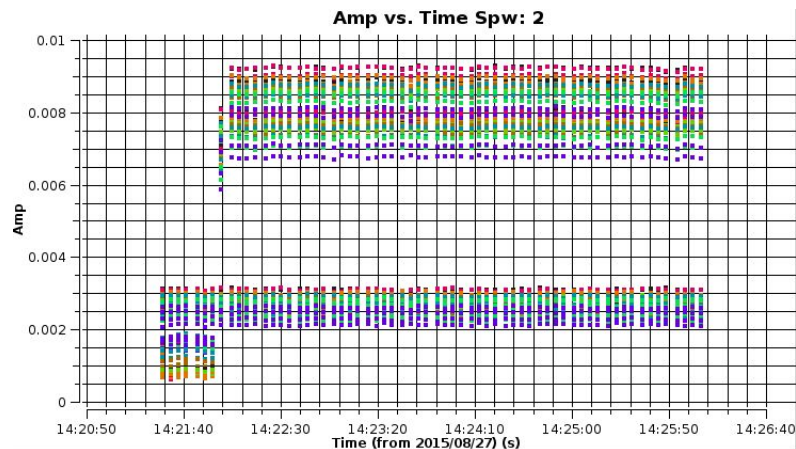
APP (**ALMA Phasing Project**) infrastructure

- **Analog Sum.**
 - In the correlator cards the analog sum is calculated.
 - 5 dedicated FPGA produces the analog sum.
 - Only correlator cards type 1 and 2 produces analog sum (they are the only ones which have access to all the antenna inputs)
- **One PPS (**P**ulse **P**er **S**econd) distributor card.**
 - This card produces and distributes copies of the 1PPS signal (generated by the Maser and GPS) to all the PICs
 - This is FA card running a custom firmware.
- **PIC (**P**hasing **I**nterface **C**ard)**
 - Makes packets (ethernet + IP + UDP + VDIF) of the analog sum data.

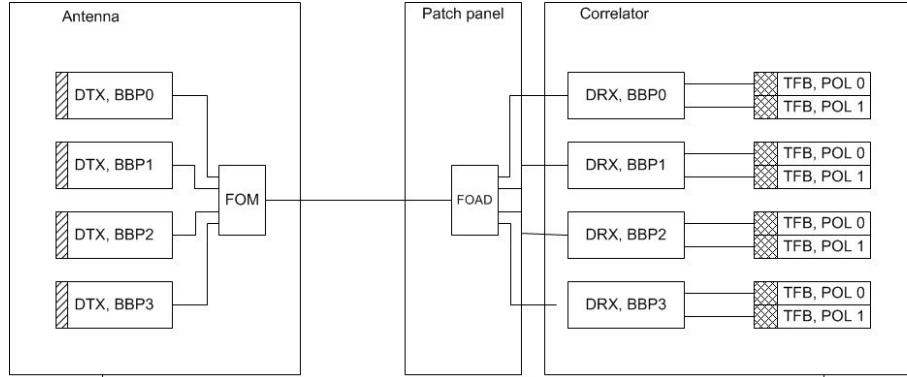
APP (ALMA Phasing Project) infrastructure



- Before adding the antennas the phase is corrected.
- Correlator software + TelCal produce phase corrections in almost real time.




Auxiliary slides




Control enables the PRN in all DTX
Within one antenna
=>

RCA=0x0C00A
Payload = 0x01
Node Ids:
0x50
0x51
0x52
0x53

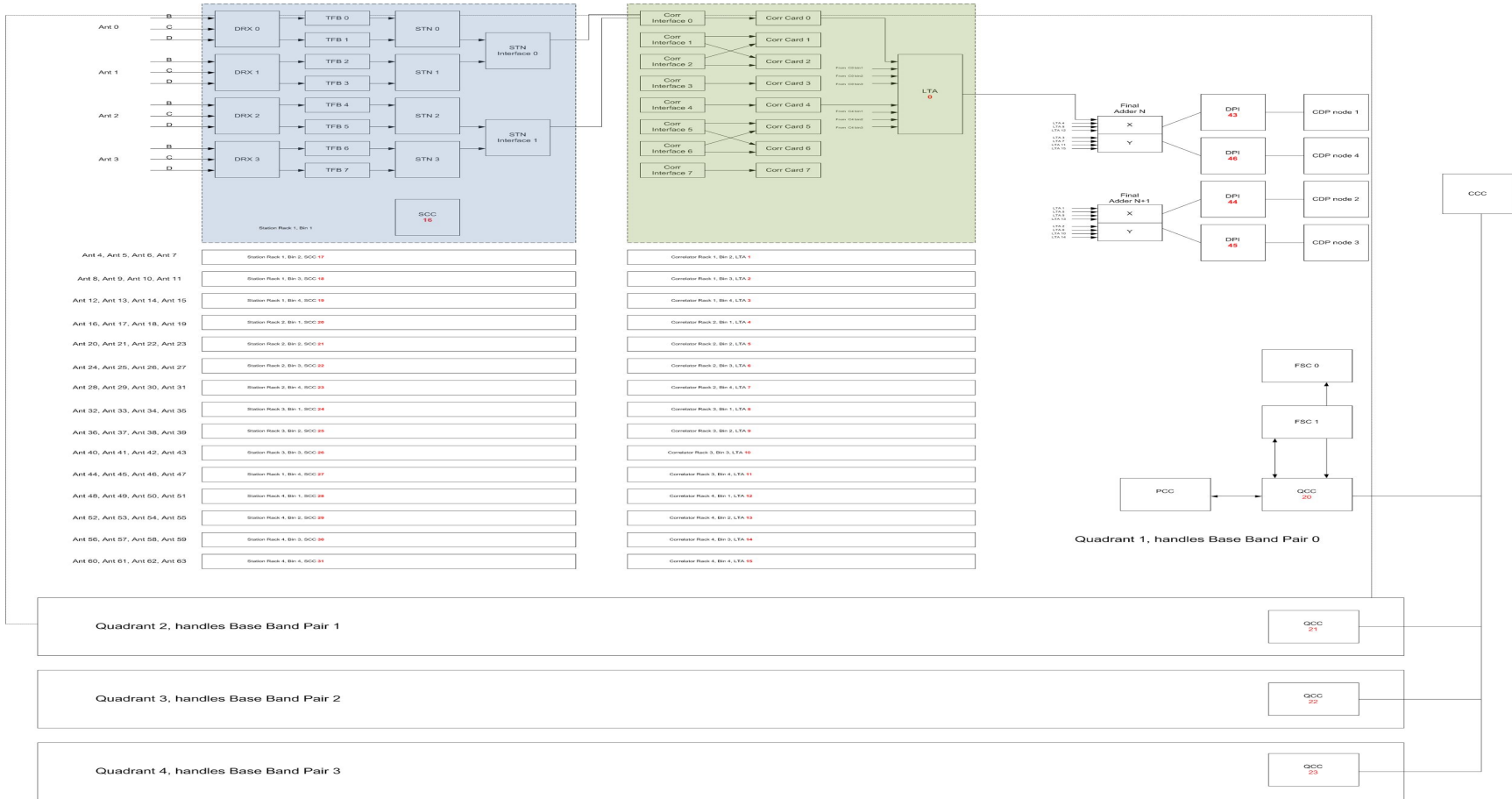
Normal mode =>
Payload = 0

 Pseudo Random
Generator

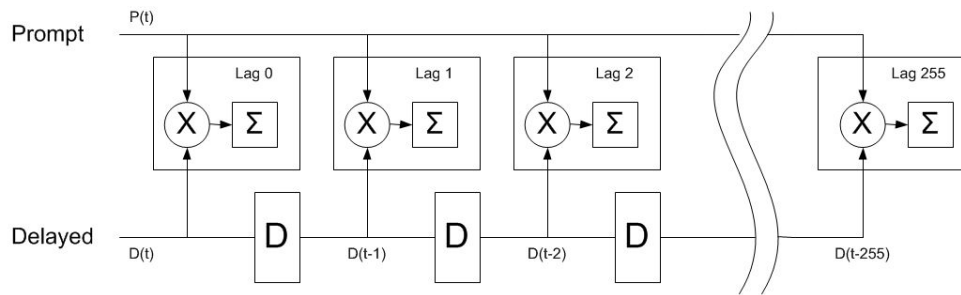
 PRN, checker

Correlator sub-system
Checks the PRN pattern in 8 TFBs
(each DRX feeds two TFBs)
"T2"

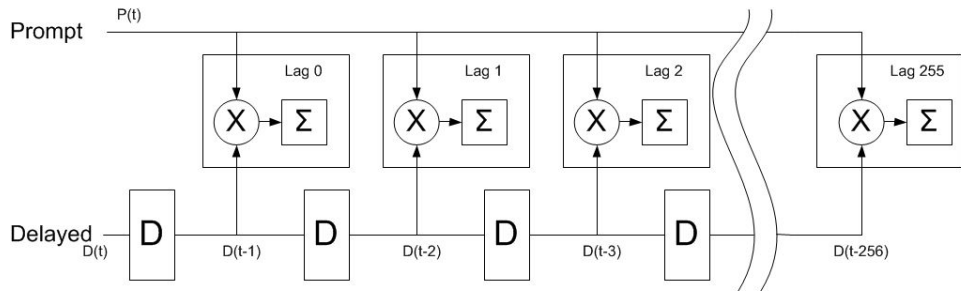
Auxiliary slide



Auxiliary slide (Intersection description)



The above figure shows how an intersection is set for "diagonal" and "lags" cases. Note that the stream of data that enters at the "delayed" input pass through a "delays" elements. Each intersection is able to produce 256 lags. When a intersections is dumped the first lag to be output is lag 0 and then lag 1 and so on until dump the 256 lags.



The above figure shows how an intersection is set for "leads" case. Note that one extra delay element is placed at the beginning of the delayed input.

Auxiliary slide (Quadrant details)

