## **Antenna Electronics Concept for the Next-Generation Very Large Array**











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d 6 A1-I 56000 Mbps prmatted to D501	Receiver and I/Q Converter / Digitizer System (Based on the proposed 6 band system as described in reference 1)	
d 6 A1-Q 56000 Mbps	The basic concept is six cryogenically cooled feeds & receivers	
d 6 A1/B1 2SB LO from L500	mounted in two dewars, covering 1.2 to 116 GHz. The signals from	
d 6 B1-I 56000 Mbps prmatted to D501	these receivers are passed into small, integrated converter / digitizer	
d 6 B1-Q 56000 Mbps prmatted to D501	devices, described in ngVLA memo 29, are based around a digitizer-	
	serializer ASIC design. They will allow common, low cost, configurable	1
d 6 A2-B2 I&Q 56000 Mbps each prmatted to D501	modules to be integrated into the receiver package. The converter/digitizer modules will produce unformatted optical data	
d 6 A2/B2 2SB LO from L500	streams to be sent off of the antenna to a local digital system at the	Band
d 6 A3-B3 I&Q 56000 Mbps each prmatted to D501	base of the antenna, or directly to the array central signal processor.	
d 6 A3/B3 2SB LO from L500 d 6 A4-B4 I&Q 56000 Mbps each	Bands 1-3 utilize the digitizers in their 8 bit 7 GS/s mode. Sky	Band
d 6 A4/B4 2SB LO from L500	frequencies from 1.2 to 10.5 GHz are direct sampled. Sky frequencies	
GHz Clk from L500	sideband separating mixers, then digitized in IQ pairs.	Band
	Bands 4.6 utiliza tha digitizars in their 4 bit 14 GS/s mode. Observable	Band
d 5 A1-I 56000 Mbps prmatted to D501	sky frequencies from 20.5 to 116 GHz are direct downconverted to	
d 5 A1-Q 56000 Mbps prmated to D501	baseband and split into IQ pairs by sideband separating mixers, then	
d 5 A1/B1 2SB LO from L500	digitized as IQ pairs.	
ormatted to D501	This system reduces the risk of LO tones polluting the signal path as is	
d 5 B1-Q 56000 Mbps prmated to D501	common in multiple conversion systems. Additionally, its simplicity ensures high gain and phase stability.	
GHz Clk from L500		Ontic
d 5 A2-B2 I&Q 56000 Mbps each prmatted to D501		optica
d 5 A2/B2 2SB LO from L500		
d 4 A-I 56000 Mbps prmatted to D501	<b>Digital Processing &amp; Transmission</b>	
d 4 A-Q 56000 Mbps	The unformatted data streams from the ADCs are optically	<u> </u>
d 4 2SB LO from L500	combined onto a smaller number of fibers. Band selection is	
d 4 B-I 56000 Mbps prmatted to D501	At the base of the antenna, or the array center, the fibers from the	LO/IF
d 4 B-Q 56000 Mbps prmatted to D501	combiners are fed into optical receivers. The outputs of the receivers	
GHz Clk from L500	are fed into clock recovery and aligner circuitry, digitally processed	
	array center for final processing. This multi-step process simplifies the	
	digital electronics and minimizes the number of RF or fiber switches in	
	monitor the system health and data integrity.	
d 3 A2-I 56000 Mbps prmatted to D501		512 MH from L50
d 3 A2-Q 56000 Mbps prmatted to D501		
d 3 2SB LO from L500 d 3 B2-I, B2-Q 56000 Mbps each	Local Oscillator/Reference System	
d 2 A3 + Band 3 A1 I 56000 Mbps prmatted to D501	The electronics at the base of the antenna receive a 512 MHz CW tone	
	and digital timing signal from the array center or a remote LO/timing	
ormatted to D501	and the source. These signals are used to lock a crystal oscillator and	
d 3 2SB LO from L500 d 2 B3 + Band 3 B1 I 56000 Mbps prmatted to D501	timing generator logic. Local Oscillator and ADC clocks are generated	
d 2 B3 + Band 3 B1 Q 56000 Mbps prmatted to D501	and sent to the front end electronics. Round trip phase of the fiber	
d 2 A2 56000 Mbps prmatted to D501	going up the antenna is also measured. This well established	
d 2 A1 56000 Mbps prmatted to D501	technique provides low jitter clock and LO signals to the ADCs and	
Hz Clk from L500 d 2 B2 56000 Mbps	reduce cost & complexity and maximize system reliability.	
ormatted to D501 d 2 B1 56000 Mbps ormatted to D501		
d 1 + Low Band A1 40000 Mbps		
	References	
d 1 + Low Band B1 40000 Mbps prmatted to D501	2 - W. Grammer, ngVLA Band Configs v4.2 (12/13/2017)	
Hz CLK from L500	3 - M. Morgan, S. Wunduke, ngVLA Memo 29: An Integrated Receiver	
	Concept for the ngVLA (11/06/17)	·





